TEXAS INSTRUMENTS
UCC57108-Q1
JAJSTC9A – DECEMBER 2023 – REVISED MARCH 2024

# UCC5710x-Q1 高速ローサイド ゲート ドライバ、DESAT 保護付き、車載用アプリケーション向け

ADVANCE INFORMATION

## 1 特長

- 車載アプリケーション認定済み
- AEC-Q100 認定済み
  - デバイス温度グレード 1
  - デバイス HBM ESD 分類レベル H1C
  - デバイス CDM ESD 分類レベル C6
- 3A シンク、3A ソース出力電流 (標準値)
- プログラマブル遅延による DESAT 保護
- フォルト発生時のソフト ターンオフ
- VDD 電圧の絶対最大値:30V
- –5V まで耐える入力およびイネーブル ピン
- 厳格な UVLO スレッショルドによりバイアスの柔軟性を確保
- 伝搬遅延時間:25ns (標準値)
- サーマル シャットダウン機能を搭載した自己保護ドライバ
- 広いバイアス電圧範囲
- 5mm × 4mm の SOIC8 パッケージで供給されます
- 動作時の接合部温度範囲:–40℃～150℃

## 2 アプリケーション

- HEV/EV PTC ヒーター
- トラクション インバータ
- 住宅用 EV チャージャ
- モーター ドライブ
- HVAC 用コンプレッサ

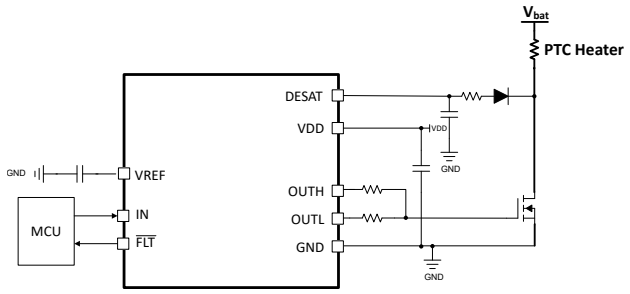
## 3 概要

UCC5710x-Q1 は、PTC ヒーター、トラクション インバータのアクティブ放電回路、その他の補助サブシステムなどの大電力車載アプリケーション向けのシングル チャネル高性能ローサイド IGBT/SiC ゲート ドライバです。低電圧誤動作防止 (UVLO)、脱飽和保護 (DESAT)、フォルト報告、サーマル シャットダウン保護などの保護機能を備えています。UCC5710x-Q1 の代表的なピーク ドライブ能力は 3A です。また、入力で -5V を扱えるため、中程度のグランド バウンスが発生するシステムの堅牢性を向上させることができます。これらの入力は電源電圧の影響を受けず、ほとんどのコントローラ出力に接続できるため、制御の柔軟性を最大限に高めることができます。異なるピン構成に応じて、UCC5710xB-Q1 で供給される広い電圧範囲のバイアス電源はバイポーラ電圧に対応します。また、ハイ / ロー ドライバ出力 (UCC5710xC-Q1) とイネーブル機能 (UCC5710xW-Q1) が提供されています。UCC5710xB-Q1 および UCC5710xC-Q1 を使用すると、正確な 5V 出力が得られます。

**パッケージ情報**

| 部品番号 | パッケージ (1) | パッケージ サイズ(2) | 本体サイズ (公称) |
|---|---|---|---|
| UCC57108B-Q1 | D (SOIC 8) | 4.9mm × 6.0mm | 4.90mm × 3.91mm |
| UCC5710xC-Q1(3) | D (SOIC 8) | 4.9mm × 6.0mm | 4.90mm × 3.91mm |
| UCC5710xW-Q1(3) | D (SOIC 8) | 4.9mm × 6.0mm | 4.90mm × 3.91mm |

(1) 供給されているすべてのパッケージについては、セクション 12 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
(3) 製品プレビュー




アプリケーション概略図

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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# 4 Pin Configuration and Functions

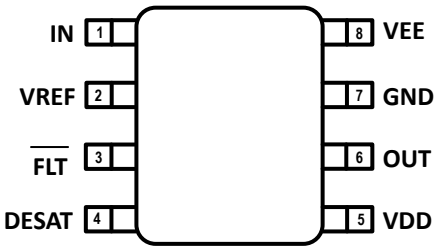


図 4-1. UCC5710xB-Q1 D Package SOIC-8 Top View

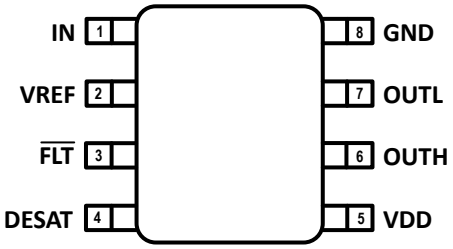


図 4-2. UCC5710xC-Q1 D Package SOIC-8 Top View

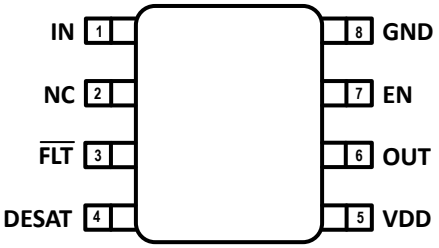


図 4-3. UCC5710xW-Q1 D Package SOIC-8 Top View

表 4-1. Pin Functions

| PIN | | | | TYPE(1) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | UCC5710xB-Q1 | UCC5710xC-Q1 | UCC5710xW-Q1 | | |
| IN | 1 | 1 | 1 | I | Non-inverting PWM input |
| VREF | 2 | 2 | NA | O | 5V Reference generated within the driver |
| NC | NA | NA | 2 | | Not Connected |
| FLTb | 3 | 3 | 3 | O | Active low fault reporting |
| DEAST | 4 | 4 | 4 | I | Input for detecting the desatuation fault |
| VDD | 5 | 5 | 5 | P | Driver bias supply |
| OUT | 6 | NA | 6 | O | Output of the driver |
| OUTH | NA | 6 | NA | O | Driver high output |
| EN | NA | NA | 6 | I | Enable or disable control pin. |
| OUTL | NA | 7 | NA | O | Driver low output |
| GND | 7 | 8 | 8 | G | Driver ground |
| VEE | 8 | NA | NA | P | Driver negtive bias supply with respect to GND |

(1) I/O = Digital input/output, IA = Analog input, AO= Analog output, P = Power connection

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# 5 Specifications

## 5.1 Absolute Maximum Ratings

All the voltages are with respect to GND. Over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| VDD-GND | Positive power supply | –0.3 | 30 | V |
| VDD-VEE | Differential Power Supply | -0.3 | 30 | V |
| VEE-GND | Negative Power Supply | -18 | 0.3 | V |
| OUT | Output signal DC voltage | GND/VEE–0.3 | VDD+0.3 | V |
| | Output signal transient voltage for 200-ns | GND/VEE–2 | VDD+3 | V |
| VDESAT | Desat voltage | –0.3 | VDD+0.3 | V |
| $V_{IN}$ | IN signal DC voltage | –5 | 30 | V |
| $V_{EN}$ | EN signal DC voltage (W Version) | –5 | 30 | V |
| $I_{\overline{FLT}}$ | $\overline{FLT}$ current sink | | 20 | mA |
| $V_{\overline{FLT}}$ | External pull-up | -0.3 | VDD+0.3 | V |
| $T_J$ | Junction temperature | –40 | 150 | ℃ |
| $T_{stg}$ | Storage temperature | –65 | 150 | ℃ |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 5.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | All pins except VREF | ±2000 | V |
| | | | VREF (UCC5710xB-Q1, UCC5710xC-Q1) | ±1500 | |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101(2) | All pins | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Thermal Information

| THERMAL METRIC(1) | | UCC5710x-Q1 D (SOIC) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 126.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 67.0 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 69.9 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 19.2 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 69.1 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.


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## 5.4 Recommended Operating Conditions

All voltages are with reference to GND. Over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VDD-GND | Positive Power Supply | UVLO | | 26 | V |
| VDD-VEE | Differential Power Supply | | | 26 | V |
| VEE-GND | Negative Power Supply | -15 | | 0 | V |
| $V_{OUT}$ | Output Voltage | GND/VEE | | VDD | V |
| $V_{IN}$ | IN signal DC voltage | -2 | | 26 | V |
| $V_{EN}$ | EN signal DC voltage (W Version) | -2 | | 26 | V |
| $T_J$ | Junction temperature | –40 | | 150 | ℃ |

## 5.5 Electrical Characteristics

VDD = 15 V, VEE = 0 V, 1-µF capacitor from VDD to GND, 1-µF capacitor from VEE to GND, TJ = –40°C to +150°C, CL = 0 pF, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENTS** | | | | | | |
| $I_{VDDQ}$ | VDD quiescent supply current | $V_{IN}$ = 3.3V, EN = 5V, VDD = 6.5V | | | 1.4 | mA |
| $I_{VDD}$ | VDD static supply current | $V_{IN}$ = 3.3 V, EN = 5V | | 1.1 | 1.5 | mA |
| $I_{VEEQ}$ | VEE static supply current | $V_{IN}$ = 0 V, EN = 5V, VEE = -10V | | | 1.1 | mA |
| $I_{VDD}$ | VDD static supply current | $V_{IN}$ = 0 V, EN = 5V | | 0.8 | 1.2 | mA |
| $I_{VDDO}$ | VDD dynamic operating current | $f_{SW}$ = 1000 kHz, EN = 5V, VDD=15 V, $C_L$=1800pF | | | 35 | mA |
| $I_{DIS}$ | VDD disable current | $V_{INx}$ = 3.3 V, EN = 0 V | | 0.8 | 1.1 | mA |
| **VDD UNDERVOLTAGE THRESHOLDS AND DELAY** | | | | | | |
| $V_{VDD_ON}$ | VDD UVLO Rising Threshold | 8.5-V UVLO Option | 7.6 | 8 | 8.4 | V |
| $V_{VDD_OFF}$ | VDD UVLO Falling Threshold | 8.5-V UVLO Option | 6.65 | 7 | 7.35 | V |
| $V_{VDD_HYS}$ | VDD UVLO Threshold Hysteresis | 8.5-V UVLO Option | | 1 | | V |
| $t_{UVLO2FLT}$ | Propagation delay from UVLO shutdown to $\overline{FLT}$ | | | 8.4 | | us |
| $V_{VDD_ON}$ | VDD UVLO Rising Threshold | 12.5-V UVLO Option | 12.8 | 13.5 | 14.2 | V |
| $V_{VDD_OFF}$ | VDD UVLO Falling Threshold | | 11.8 | 12.5 | 13.2 | V |
| $V_{VDD_HYS}$ | VDD UVLO Threshold Hysteresis | | | 1.0 | | V |
| **VREF** | | | | | | |
| $V_{REF}$ | Voltage Reference | $I_{REF}$=10mA | | 5 | | V |
| $I_{REF}$ | Reference output current | | | | 20 | mA |
| **IN, EN** | | | | | | |
| $V_{INH}$ | Input High Threshold Voltage | Output goes high when threshold is reached | 1.8 | 2.2 | 2.6 | V |
| $V_{INL}$ | Input Low Threshold Voltage | Output goes low when threshold reached | 0.8 | 1.2 | 1.6 | V |
| $V_{IN_HYS}$ | Input-threshold Hysteresis | Calculate as $V_{INH}$ - $V_{INL}$ | | 1.0 | | V |
| $R_{IND}$ | IN Pin Pull Down Resistance | IN, DIS = 3.3V | | 120 | | kΩ |
| $V_{ENH}$ | Enable High Threshold Voltage | Output goes HIGH when threshold reached | 1.8 | 2.2 | 2.6 | V |
| $V_{ENL}$ | Enable Low Threshold Voltage | Output goes LOW when threshold reached | 0.8 | 1.2 | 1.6 | V |
| $V_{EN_HYS}$ | Enable Threshold Hysteresis | Calculate as $V_{ENH}$ - $V_{ENL}$ | | 1 | | V |
| $R_{ENU}$ | EN Pin Pull Up Resistance | EN = 0V | | 400 | | kΩ |
| $V_{FLTth}$ | $\overline{FLT}$ threshold voltage | $I_{FLT\text{-}sink}$ = 15mA | | 0.43 | 1 | V |

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## 5.5 Electrical Characteristics (続き)

VDD = 15 V, VEE = 0 V, 1-µF capacitor from VDD to GND, 1-µF capacitor from VEE to GND, TJ = –40°C to +150°C, CL = 0 pF, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DESAT DETECTION** | | | | | | |
| $I_{CHG}$ | Blanking capacitor charge current (250µA variant) | $V_{DESAT}$ = 3.25V | 200 | 250 | 316 | µA |
| $I_{DCHG}$ | DESAT pin discharge current | $V_{DESAT}$ = 8V | | -20 | | mA |
| $V_{DESATTH}$ | DESAT Detection Threshold | $\overline{FLT}$ goes low when threshold is reached | 6.0 | 6.5 | 7.0 | V |
| $V_{DESLO}$ | DESAT voltage when OUT=L, referenced to GND | | | | 100 | mV |
| $t_{DESLEB}$ | Leading edge blanking time | | | 150 | | ns |
| $t_{DESFIL}$ | DESAT deglitch filter | | | 100 | 150 | ns |
| $t_{DES2OUT}$ | DESAT propagation delay to 90% of OUT | $V_{DESAT}$>$V_{DESATTH}$ | | 140 | 250 | ns |
| $t_{DES2FLT}$ | DESAT propagation delay to $\overline{FLT}$ low | $V_{DESATTH}$ to 90% of $\overline{FLT}$, Cl=10pF | | 135 | 250 | ns |
| **SOFT TURN OFF** | | | | | | |
| $R_{STO}$ | Internal Soft turn-off Pulldown Resistance | DESAT triggered, $V_{OUT}$=5V | | 35 | | Ω |
| **OVERTEMPERATURE PROTECTION** | | | | | | |
| $T_{SD}$ | Overtemperature threshold | | | 180 | | C |
| $T_{HYS}$ | Overtemperature protection hysteresis | | | 30 | | C |
| $t_{OTP2FLT}$ | Propagation delay from overtemperature shutdown to $\overline{FLT}$ | Over temperature shutdow to 90% of $\overline{FLT}$, Cl=10pF | | 8 | | us |
| **OUTPUT DRIVER STAGE** | | | | | | |
| $I_{SRCPK}$ | Peak Output Source Current | $C_{VDD}$ = 10 µF, $C_L$ = 0.1 µF, f = 1 kHz | | -3 | | A |
| $I_{SNKPK}$ | Peak Output Sink Current | $C_{VDD}$ = 10 µF, $C_L$ = 0.1 µF, f = 1 kHz | | 2.8 | | A |
| $R_{OH}$ | Pull up resistance | $I_{OUT}$ = –500mA | | 5 | | Ω |
| $R_{OL}$ | Pull down resistance | $I_{OUT}$ = 500mA | | 1 | | Ω |

## 5.6 Switching Characteristics

VDD = 15 V, VEE = 0 V, 1-µF capacitor from VDD to GND, 1-µF capacitor from VEE to GND, TJ = –40°C to +150°C, CL = 0 pF, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{RA}$, $t_{RB}$ | Output Rise Time | $C_L$=1.8nF, 10% to 90%, Vin = 0 to 3.3V | | 8 | 18 | ns |
| $t_{FA}$, $t_{FB}$ | Output Fall Time | $C_L$=1.8nF, 90% to 10%, Vin = 0 to 3.3V | | 14 | 32 | ns |
| $t_{D2}$ | Propagation Delay – Input falling to output falling | $C_L$=1.8nF, from 1V falling on Vin to 90% of output fall, Vin=0 - 3.3V, Fsw=500kHz, 50% duty cycle | | 28 | 50 | ns |
| $t_{D1}$ | Propagation Delay – Input rising to output rising | $C_L$=1.8nF, from 2V rising on Vin to 10% of output rise, Vin=0 - 3.3V, Fsw=500kHz, 50% duty cycle | | 26 | 50 | ns |
| $t_{PD_EN}$ | EN Response Delay (W Version) | $C_L$=1.8nF, from 2V rising on EN to 10% of output rise, EN=0 - 3.3V, Fsw=500kHz, 50% duty cycle | | 26 | 40 | ns |
| $t_{PD_DIS}$ | DIS Response Delay (W Version) | $C_L$=1.8nF, from 1V falling on EN to 90% of output fall, EN=0 - 3.3V, Fsw=500kHz, 50% duty cycle | | 27 | 45 | ns |
| $t_{PWmin}$ | Minimum Input Pulse Width That Passes to Output | $C_L$=1.8nF, Vin=0 - 3.3V, Fsw=500kHz, Vo >2V | | 9 | 15 | ns |

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### 5.6 Switching Characteristics (続き)

VDD = 15 V, VEE = 0 V, 1-µF capacitor from VDD to GND, 1-µF capacitor from VEE to GND, TJ = –40°C to +150°C, CL = 0 pF, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PWD}$ | Pulse Width Distortion | Input Pulse Width = 100ns, 500kHz<br>$t_{D2_1} - t_{D1_1}$ ,$C_L$=1.8nF | -10 | | 10 | ns |

## 6 Detailed Description

### 6.1 Overview

The UCC5710x-Q1 deviceis a single-channel, high-speed, gate drivers capable of effectively driving MOSFET, SiC MOSFET, and IGBT power switches with 3-A source and 3-A sink (symmetrical drive) peak current. The driver has a good transient handling capability on its output due to reverse currents, as well as rail-to-rail drive capability and small propagation delay, typically 26ns. The device has the state-of-art DESAT detection time, and fault reporting function to the low voltage side DSP/MCU. Soft turn off is triggered when the DESAT fault is detected, minimizing the short circuit energy while reducing the overshoot voltage on the switch.

The input threshold of UCC5710x-Q1 is compatible to TTL low-voltage logic, which is fixed and independent of VDD supply voltage. The driver can also work with CMOS based controllers as long as the threshold requirement is met. The 1-V typical hysteresis offers excellent noise immunity.

In the UCC5710xW-Q1, the driver has an EN pin with fixed TTL compatible threshold. EN is internally pulled up.Pulling EN low disables the driver, while leaving EN open provides normal operation. In the UCC5710xB-Q1 and UCC5710xC-Q1 offer an additional 5V output (VREF) that source up to 20mA function.

### 6.2 Functional Block Diagram

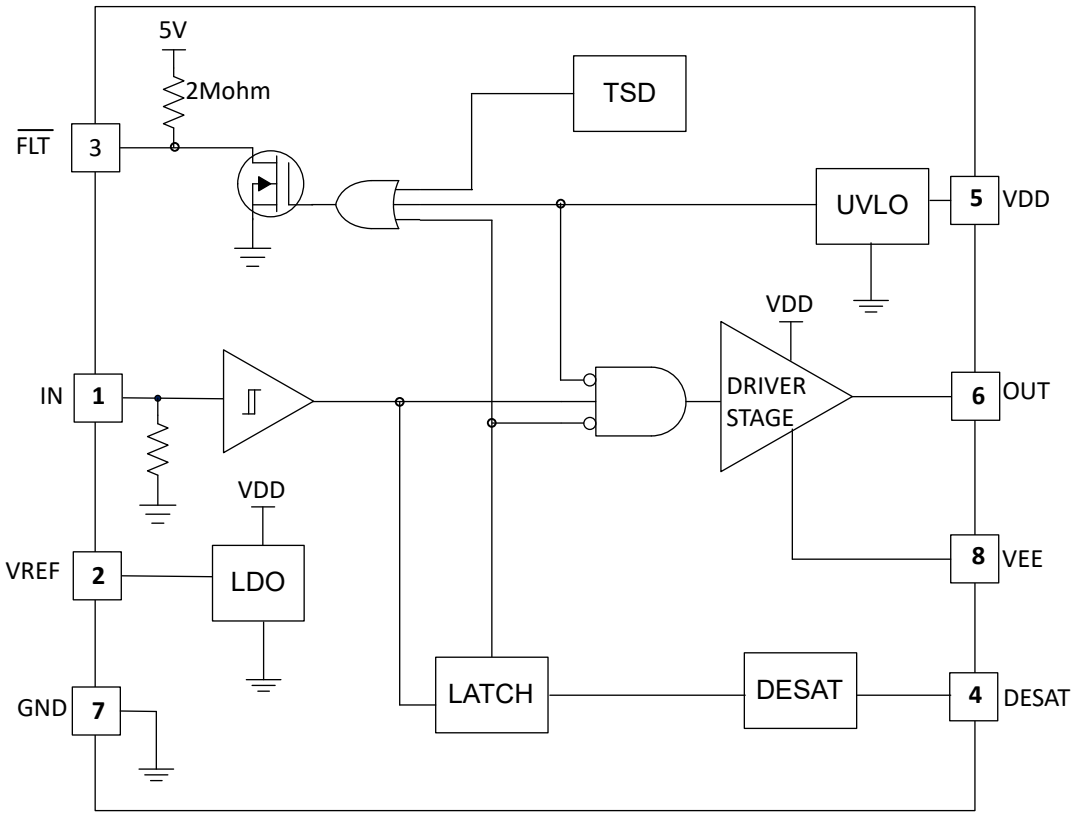


**図 6-1. UCC5710xB-Q1 Simplified Functional Block Diagram**

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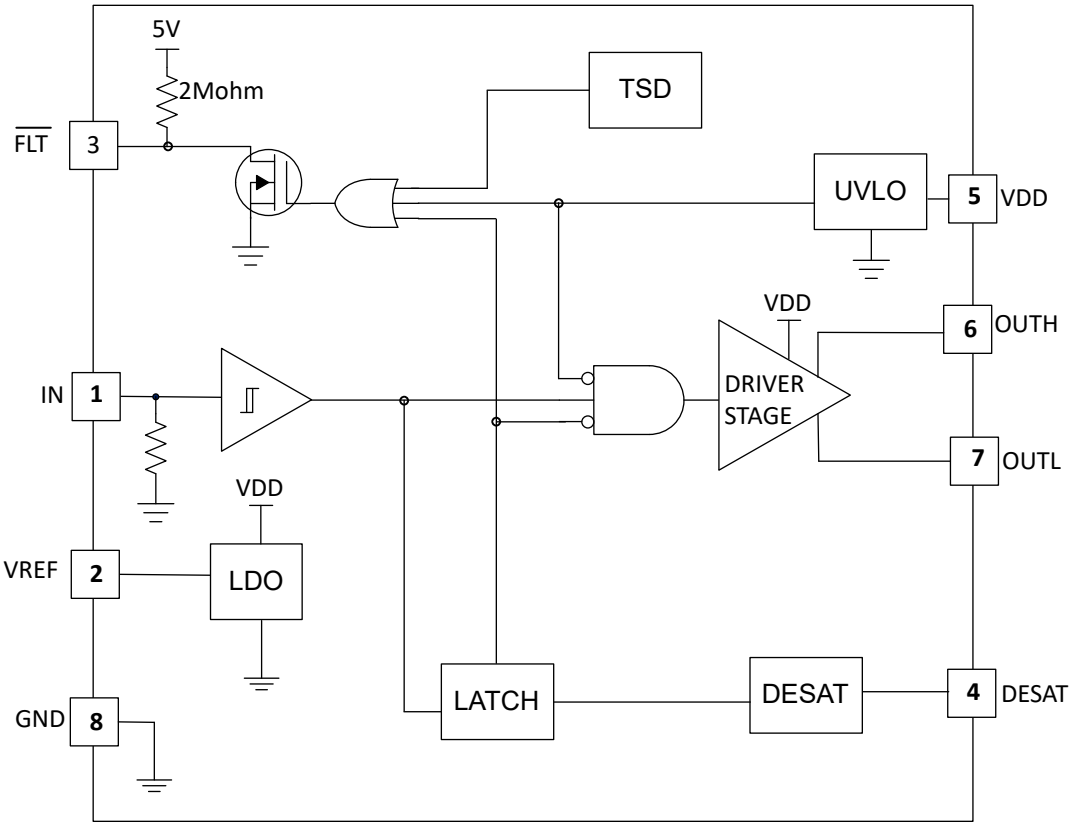


**図 6-2. UCC5710xC-Q1 Simplified Functional Block Diagram**


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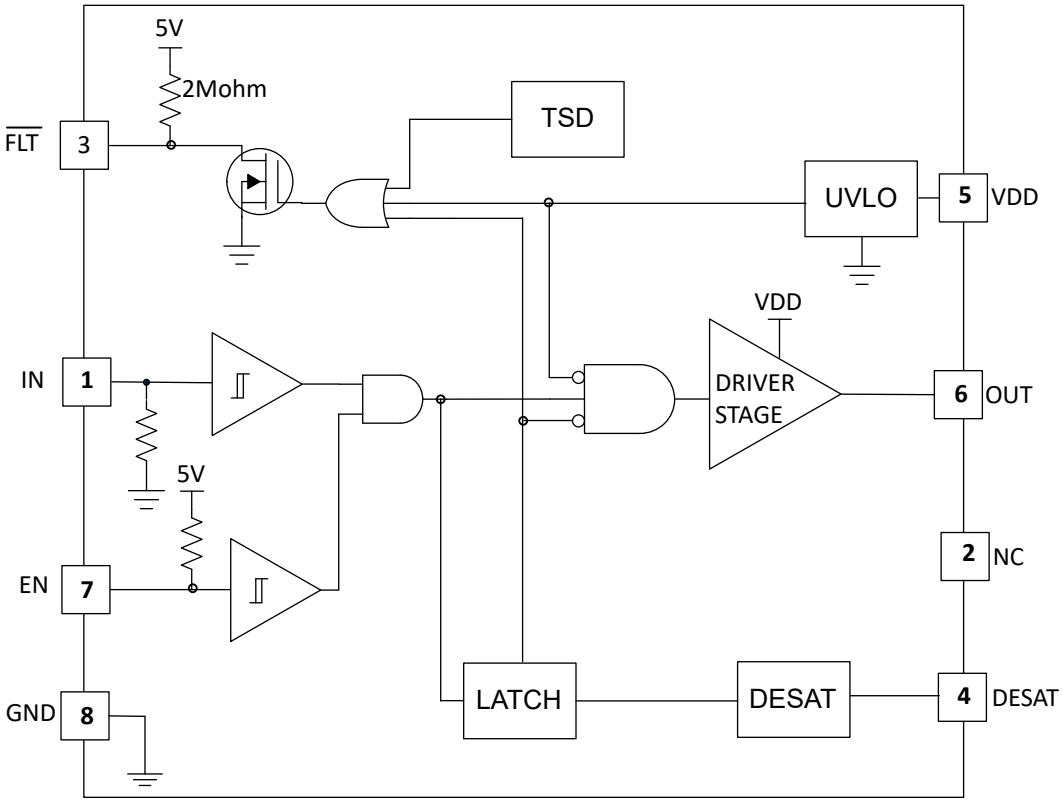


**図 6-3. UCC5710xW-Q1 Simplified Functional Block Diagram**

## 6.3 Feature Description

### 6.3.1 Input Stage

The inputs of the UCC5710x-Q1 device are compatible with TTL based threshold logic andthe inputs are independent of the VDD supply voltage. With typical high threshold of 2.2 V and typical low threshold of 1.2 V, the logic level thresholds can be conveniently driven with PWM control signals derived from 3.3-V or 5-V logic. Wider hysteresis (typically 1 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. This device also features tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature. The very low input capacitance, typically less than 8 pF, on these pins reduces loading and increases switching speed.

The device features an important protection function wherein, whenever the input pin is in a floating condition, the output is held in the low state. This is achieved with internal pullup or pulldown resistors on the input pins as shown in the simplified functional block diagrams. In some applications, due to difference in bias supply sequencing, different ICs power-up at different times. This may cause output of the controller to be in tri-state. This output of the controller gets connected to the input of the driver IC. If the driver IC does not have a pulldown resistor then the output of the driver may go high erroneously and damage the switching power device.

The input stage of the driver should preferably be driven by a signal with a short rise or fall time. Caution must be exercised whenever the driver is used with slowly varying input signals, especially in situations where the device is located in a separate daughter board or PCB layout has long input connection traces:

- High dI/dt current from the driver output coupled with board layout parasitics can cause ground bounce. Because the device features just one GND pin which may be referenced to the power ground, this may interfere with the differential voltage between Input pins and GND and trigger an unintended change of output state. Because of fast 26-ns propagation delay, this can ultimately result in high-frequency oscillations, which increases power dissipation and poses risk of damage.

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- 1-V Input threshold hysteresis boosts noise immunity compared to most other industry standard drivers.

An external resistance is highly recommended between the output of the driver and the power device instead of adding delays on the input signal. This also limits the rise or fall times to the power device which reduces the EMI. The external resistor has the additional benefit of reducing part of the gate charge related power dissipation in the gate driver device package and transferring it into the external resistor itself.

Finally, because of the unique input structure that allows negative voltage capability on the Input and Enable pins, caution must be used in the following applications:

- Input or Enable pins are switched to amplitude > 15 V.
- Input or Enable pins are switched at dV/dt > 2 V/ns.

If both of these conditions occur, add a series 150-Ω resistor for the pin(s) being switched to limit the current through the input structure.

### 6.3.2 Enable Function

The Enable (EN) pin of the UCC5710xW-Q1 device also has TTL compatible input thresholds with wide hysteresis. The typical turnon threshold is 2.2V and the typical turn-off threshold is 1.2V with typical hysteresis of 1V. The Enable (EN) pin of the UCC5710xW-Q1 has an internal pullup resistor to an internal reference voltage. Thus, leaving the Enable pin floating turns on the driver and allows it to send output signals properly. If desired, the Enable can also be driven by low-voltage logic to enable and disable the driver. There is minimum delay from the enable block to the output for fast system response time. Similar to the input pins, the enable pin can also handle significant negative voltage and therefore provides system robustness. The enable pin can withstand wide range of slew rate such as 1V/ns to 1V/ms. The enable signal is independent of VDD voltage and stable across the full operating temperature range.

### 6.3.3 Driver Stage

The device has ±3-A peak drive strength and is suitable for driving IGBT/SiC. The driver features an important safety function wherein, when the input pins are in floating condition, the output is held in LOW state. The driver has rail-to-rail output by implementing an NMOS pull-up with intrinsic bootstrap gate drive. Under DC conditions, a PMOS is used to keep OUT tied to VDD as shown in the figure. The low pullup impedance of the NMOS results in strong drive strength during the turn-on transient, which shortens the charging time of the input capacitance of the power semiconductor and reduces the turn on switching loss.

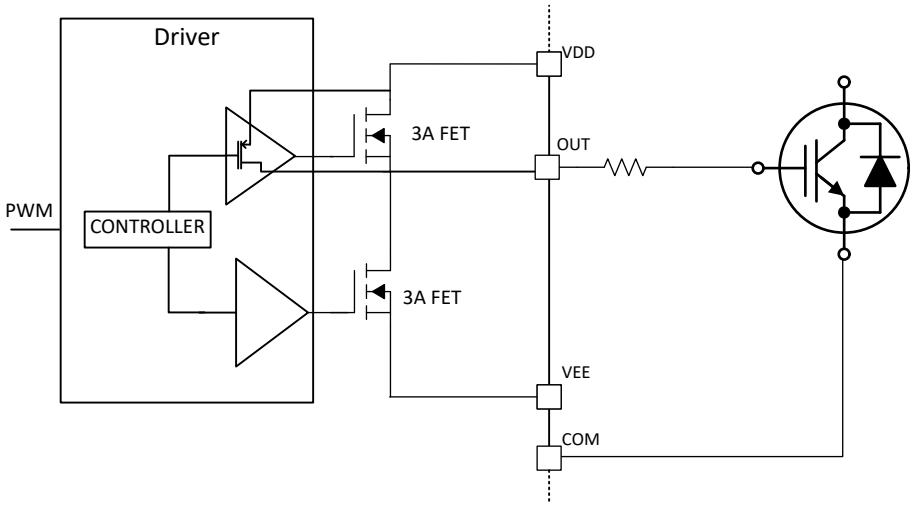


**図 6-4. Gate Driver Output Stage**

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### 6.3.4 Desaturation (DESAT) Protection

The UCC5710x-Q1 implements a fast overcurrent and short circuit protection feature to protect the MOSFET/IGBT from catastrophic breakdown during fault. The DESAT pin has a typical 6.5 V threshold with respect to COM, the source or emitter of the power semiconductor. When the input is in a floating condition or the output is held in low state, the DESAT pin is pulled down by an internal MOSFET and held in the LOW state, which prevents the overcurrent and short circuit fault from false triggering. The internal current source of the DESAT pin is activated only during the driver ON state, which means the overcurrent and short circuit protection feature only works when the power semiconductor is in the ON state. The internal pulldown MOSFET helps to discharge the voltage of the DESAT pin when the power semiconductor is turned off. The features a 150-ns internal leading edge blanking time after the OUT switches to high state. The UCC5710x-Q1 internal current source is activated to charge the external blanking capacitor after the internal leading edge blanking time. The typical value of the internal current source is 250 µA.

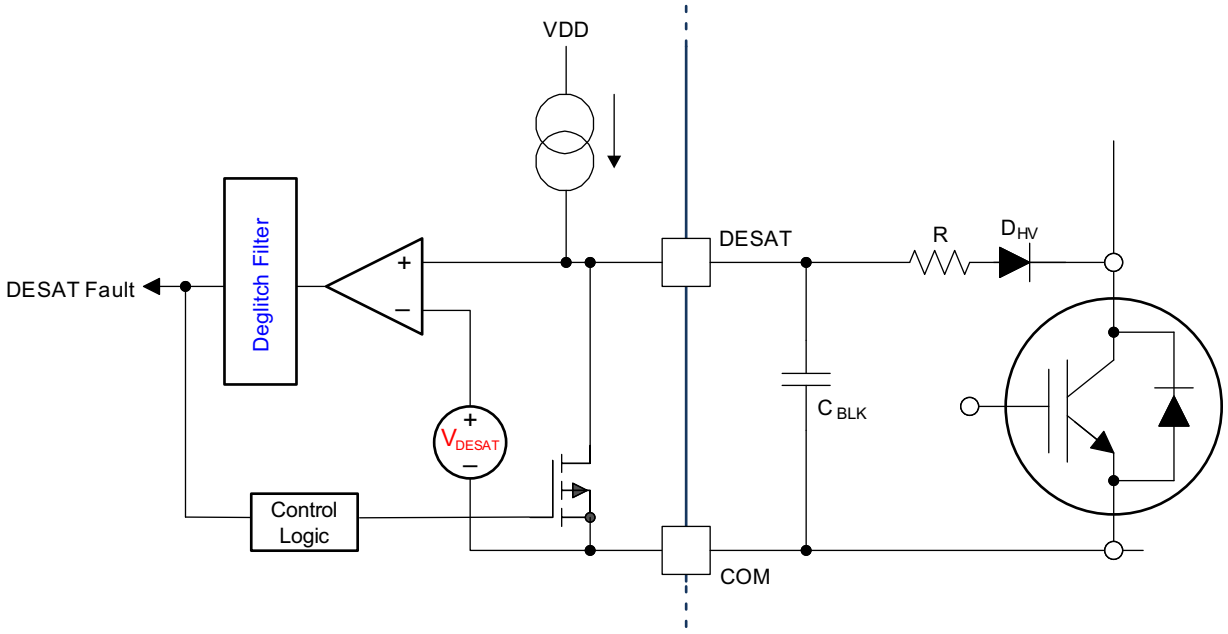


**図 6-5. DESAT Protection**

### 6.3.5 Fault ($\overline{FLT}$)

The $\overline{FLT}$ pin of UCC5710x-Q1 can report a fault signal to the DSP/MCU when the fault is detected through the DESAT pin, internal TSD or the UVLO. The $\overline{FLT}$ pin is pulled down to GND after the fault is detected, and is held low until the fault is clear.

## 6.4 Device Functional Modes

The UCC5710x-Q1 devices operate in normal mode and UVLO mode (see セクション 7.2.2.1 for information on UVLO operation). In normal mode, the output state is dependent on the states of the device, and the input pins.

The UCC5710xW-Q1 features a single, non-inverting input, but also contains enable and disable functionality through the EN pin. Setting the EN pin to logic HIGH will enable the non-inverting input to output on the IN pin.

**表 6-1. UCC5710xB-Q1, UCC5710xC-Q1 Truth Table**

| IN | DESAT | INTERNAL TSD | $\overline{FLT}$ | OUT |
|---|---|---|---|---|
| H | L | L | Open drain | H |
| L | L | L | Open drain | L |
| H | H | L | L | L |

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表 6-1. UCC5710xB-Q1, UCC5710xC-Q1 Truth Table (続き)

| IN | DESAT | INTERNAL TSD | $\overline{FLT}$ | OUT |
|---|---|---|---|---|
| X | X | H | L | L |

表 6-2. UCC5710xW-Q1 Truth Table

| IN | EN | DESAT | INTERNAL TSD | $\overline{FLT}$ | OUT |
|---|---|---|---|---|---|
| L | H | L | L | Open drain | L |
| H | H | L | L | Open drain | H |
| X | L | X | X | X | L |
| H | H | H | L | L | L |
| X | H | X | H | L | L |

# 7 Applications and Implementation

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## 7.1 Application Information

High-current gate driver devices are required in switching power applications for a variety of reasons. To enable fast switching of power devices and reduce associated switching power losses, a powerful gate driver can be employed between the PWM output of controllers or signal isolation devices and the gates of the power semiconductor devices. Further, gate drivers are indispensable when sometimes it is just not feasible to have the PWM controller directly drive the gates of the switching devices. The situation will be often encountered because the PWM signal from a digital controller or signal isolation device is often a 3.3-V or 5-V logic signal which is not capable of effectively turning on a power switch. A level-shifting circuitry is needed to boost the logic-level signal to the gate-drive voltage in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar, (or P- N-channel MOSFET), transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate for this because they lack level-shifting capability and low-drive voltage protection. Gate drivers effectively combine both the level-shifting, buffer drive and UVLO functions. Gate drivers also find other needs such as minimizing the effect of switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself.

The UCC5710x-Q1 is very flexible in this role with a strong drive current capability and wide recommended supply voltage range of UVLO to 26 V. This allows the driver to be used in 5-V bias logic level very high frequency MOSFET applications, 12-V MOSFET applications, 20-V and -5-V (relative to Source) SiC FET applications, 15-V and -8-V (relative to Emitter) IGBT applications and many others.

These requirements, coupled with the need for low propagation delays and availability in compact, and low-inductance packages with good thermal capability, make gate driver devices such as the UCC5710x-Q1 extremely important components in switching power combining benefits of high-performance, low cost, low component count, board space reduction and simplified system design.

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## 7.2 Typical Application

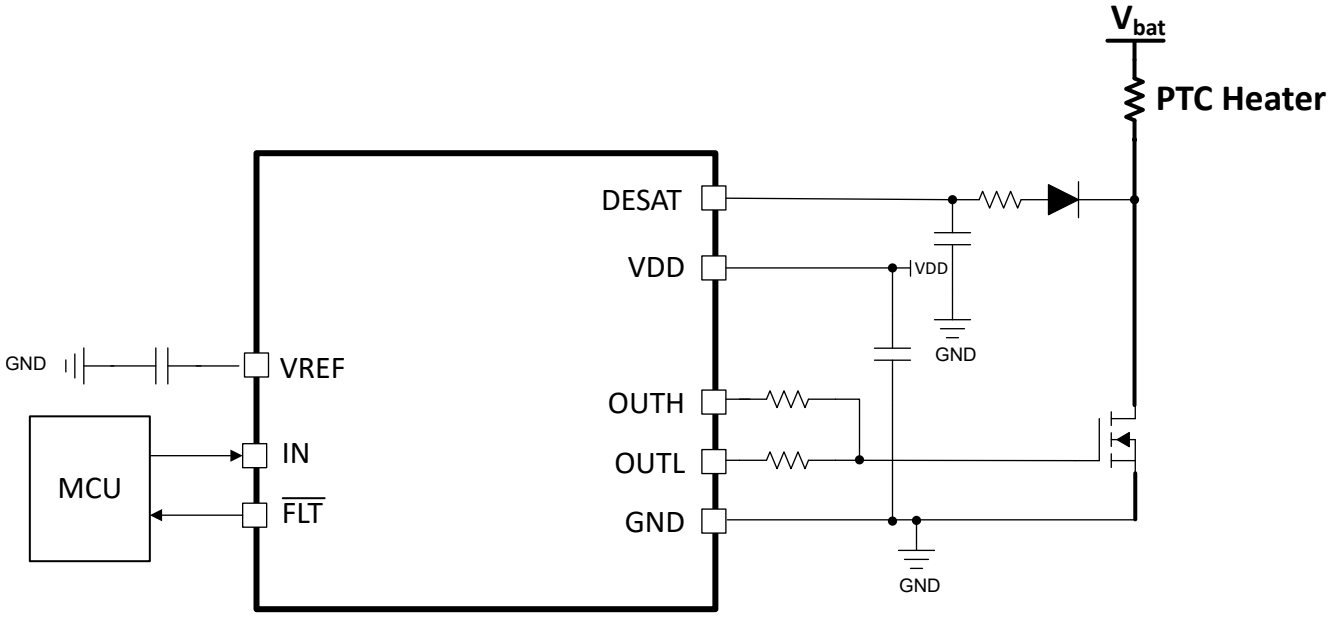


**図 7-1. UCC57108C-Q1 Used in a PTC Heater Application**

### 7.2.1 Design Requirements

When selecting the gate driver device for an end application, some design considerations must be evaluated in order to make the most appropriate selection. Following are some of the design parameters that should be used when selecting the gate driver device for an end application: input-to-output configuration, the input threshold type, bias supply voltage levels, peak source and sink currents, availability of independent enable and disable functions, propagation delay, power dissipation, and package type. See the example design parameters and requirements in 表 7-1.

**表 7-1. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Input to output logic | Non-inverting |
| Input threshold type | TTL |
| Bias supply voltage levels | +18 V |
| Negative output low voltage | N/A |
| $dV_{DS}/dt$ (1) | 100 V/ns |
| Enable function | Yes |
| Disable function | N/A |
| Propagation delay | <30 ns |
| Power dissipation | <1 W |
| Package type | SON8 or SOIC8 |

(1) $dV_{DS}/dt$ is a typical requirement for a given design. This value can be used to find the peak source/sink currents needed as shown in .

### 7.2.2 Detailed Design Procedure

#### *7.2.2.1 VDD Undervoltage Lockout*

The UCC57108-Q1 device offers an undervoltage lockout threshold of 8 V and UCC57102 provide under voltage lockout threshold of 12V. The device's hysteresis range helps to avoid any chattering due to the presence of

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noise on the bias supply. 1V of typical UVLO hysteresis is expected. There is no significant driver output turnon delay due to the UVLO feature, and 4 µs of UVLO delay is expected. The UVLO turn-off delay is also minimized as much as possible. The UVLO delay is designed to minimize chattering that may occur due to very fast transients that may appear on VDD. When the bias supply is below UVLO thresholds, the outputs are held actively low irrespective of the state of input pins and enable pin. The device accepts a wide range of slew rates on its VDD pin, and VDD noise within the hysteresis range does not affect the output state of the driver (neither ON nor OFF).

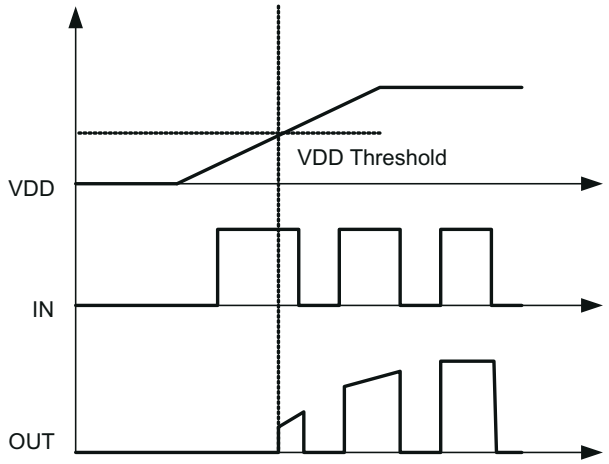


**図 7-2. Power Up**

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### 7.2.3 Application Curves

The figures below show the typical switching characteristics of the UCC57108-Q1 device with a 1nF capacitor load.

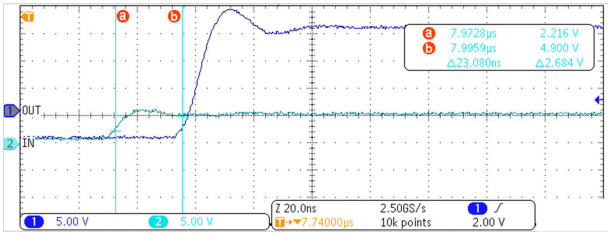


**図 7-3. UCC57108-Q1 Rising (Turn-On) Propagation Delay**

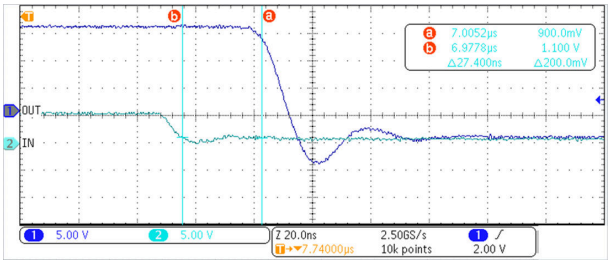


**図 7-4. UCC57108-Q1 Falling (Turn-Off) Propagation Delay**

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## 8 Power Supply Recommendations

The bias supply voltage range for which the UCC5710x-Q1 devices are recommended to operate is from UVLO to 26 V. The lower end of this range is governed by the internal UVLO protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition when the VDD pin voltage is below the $V_{(ON)}$ supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 26-V recommended maximum voltage rating of the VDD pin of the device. The absolute maximum voltage for the VDD pin is 30 V.

The UVLO protection feature also involves a hysteresis function. This means that when the VDD pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification. Therefore, ensuring that, while operating at or near the UVLOrange, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown.

During system shutdown, the device operation continues until the VDD pin voltage has dropped below the VDD UVLO falling threshold which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system start-up, the device does not begin operation until the VDD pin voltage has exceeded above the VDD UVLO rising threshold. The quiescent current consumed by the internal circuit blocks of the device is supplied through the VDD pin. Although this fact is well known, recognizing that the charge for source current pulses delivered by the OUT pin is also supplied through the same VDD pin is important. As a result, every time a current is sourced out of the output pin (OUT), a corresponding current pulse is delivered into the device through the VDD pin. Thus ensuring that local bypass capacitors are provided between the VDD and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low-ESR, ceramic surface-mount capacitor is needed. TI recommends having two capacitors; a 100-nF ceramic surface-mount capacitorplaced less than 1mm from the VDD pin of the device and another ceramic surface-mount capacitor of few microfarads added in parallel.

UCC5710x-Q1 is a high current gate driver. If the gate driver is placed far from the switching power device such as MOSFET then that may create large inductive loop. Large inductive loop may cause excessive ringing on any and all pins of the gate driver. This may result in stress exceeding device recommended rating. Therefore, it is recommended to place the gate driver as close to the switching power device as possible. It is also advisable to use an external gate resistor to damp any ringing due to the high switching currents and board parasitic elements.

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# 9 Layout

## 9.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current, fast-switching circuit to provide appropriate device operation and design robustness. The UCC5710x-Q1 gate driver incorporates short propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power switch to facilitate voltage transitions very quickly. Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are recommended when designing with these high-speed drivers.

- Place the driver device as close as possible to power device to minimize the length of high-current traces between the driver output pins and the gate of the power switch device.
- Place the bypass capacitors between VDD pin and the GND pin as close to the driver pins as possible to minimize trace length for improved noise filtering. TI recommends having two capacitors; a 100-nF ceramic surface-mount capacitor placed less than 1mm from the VDD pin of the device and another ceramic surface-mount capacitor of few microfarads added in parallel. These capacitors support high peak current being drawn from VDD during turnon of power switch. The use of low inductance surface-mount components such as chip capacitors is highly recommended.
- The turnon and turn-off current loop paths (driver device, power switch and VDD bypass capacitor) should be minimized as much as possible in order to keep the stray inductance to a minimum. High di/dt is established in these loops at two instances – during turnon and turn-off transients, which induces significant voltage transients on the output pins of the driver device and gate of the power switch.
- Wherever possible, parallel the source and return traces of a current loop, taking advantage of flux cancellation
- Separate power traces and signal traces, such as output and input signals.
- To minimize switch node transients and ringing, adding some gate resistance and/or snubbers on the power devices may be necessary. These measures may also reduce EMI.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as source of power switch, ground of PWM controller, and so forth, at a single point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT pin may corrupt the input signals during transitions. The ground plane must not be a conduction path for any current loop. Instead the ground plane should be connected to the star-point with one trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.

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## 9.2 Layout Example

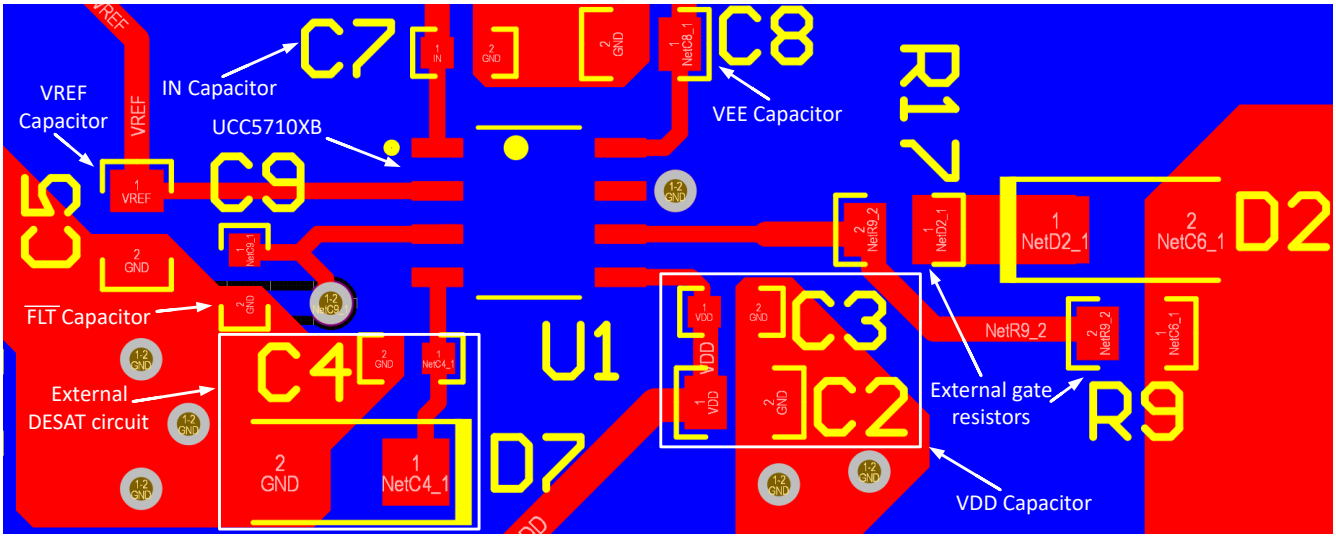


**図 9-1. Layout Example: UCC5710xB-Q1**

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# 10 Device and Documentation Support

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# 11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision * (December 2023) to Revision A (March 2024) | Page |
|---|---|
| • UCC57108B-Q1 公開事前情報のリリース | 1 |

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PUCC57108BQDRQ1 | ACTIVE | SOIC | D | 8 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |

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**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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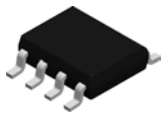
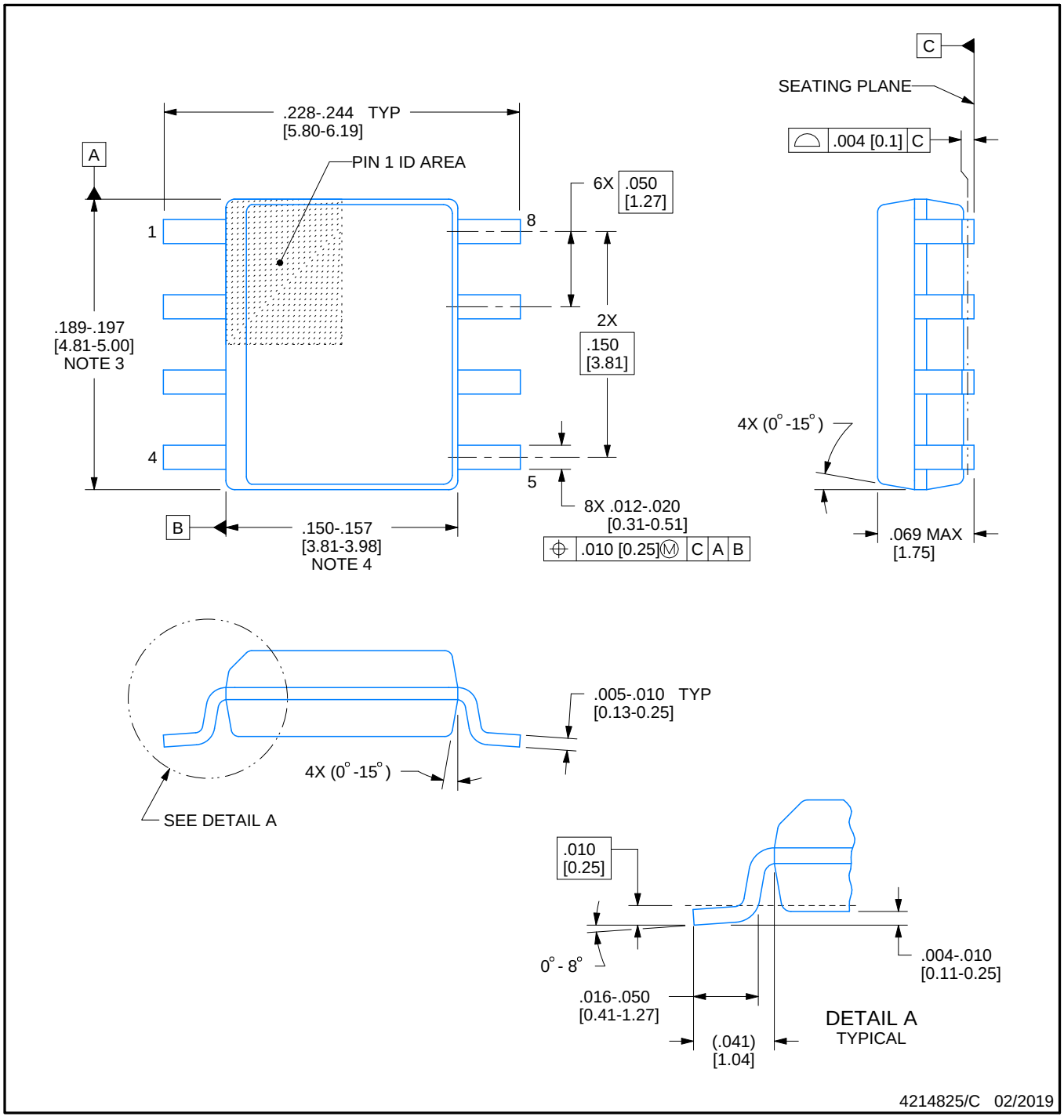


# PACKAGE OUTLINE

## D0008A

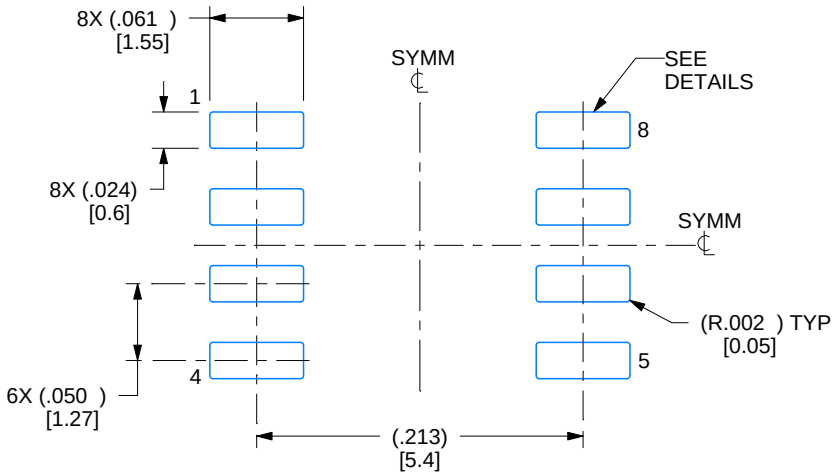
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

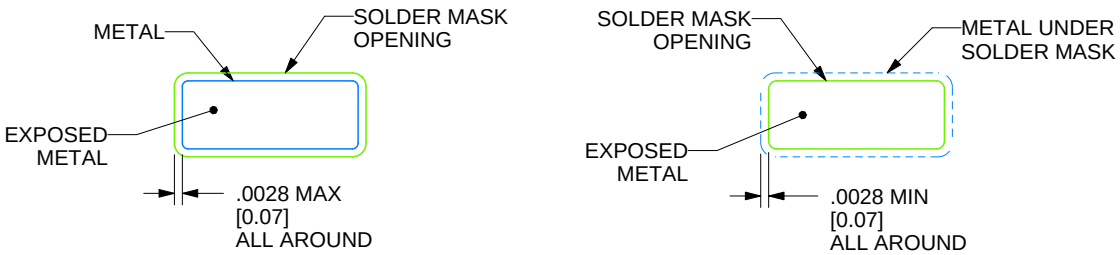



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

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NOTES: (continued)

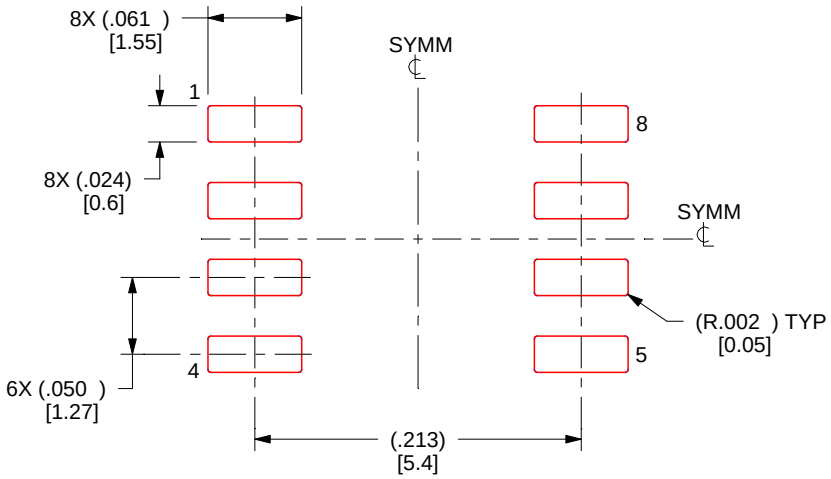
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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