TEXAS INSTRUMENTS
OPA3S2859-EP
JAJSKN5B – APRIL 2021 – REVISED DECEMBER 2021

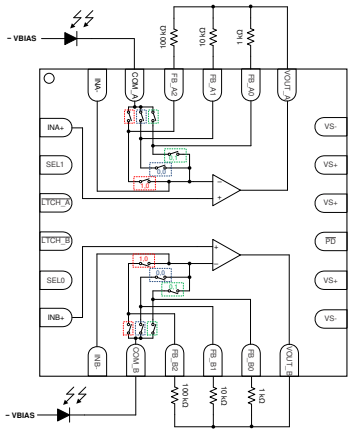
OPA3S2859-EP エンハンスド製品、デュアルチャネル、900MHz、2.2nV/√Hz、プログラマブル・ゲイン・トランスインピーダンス・アンプ

1 特長

- ゲイン帯域幅積:900MHz
- 内部スイッチでゲインをプログラム可能
- 高インピーダンスの FET 入力
- 入力電圧ノイズ:2.2nV/√Hz
- スルーレート:350V/µs
- 電源電圧範囲:3.3V～5.25V
- 静止電流:22 mA/チャネル
- パワーダウン・モードの I_Q:75µA
- 温度範囲:-55℃～125℃
- 防衛、航空宇宙、および医療アプリケーションをサポート
  - 管理されたベースライン
  - 単一のアセンブリ/テスト施設
  - 単一の製造施設
  - 長い製品ライフ・サイクル
  - 製品変更通知期間の延長
  - 製品のトレーサビリティ

2 アプリケーション

- スイッチャブル・トランスインピーダンス・アンプ
- スマート軍需品
- レーザーによる測距
- 光学時間領域反射率測定 (OTDR)
- シリコン・フォトマルチプライヤ (SiPM) バッファ
- フォトマルチプライヤ管のポスト・アンプ
- 高速プログラマブル・ゲイン・アンプ



ブロック図

3 概要

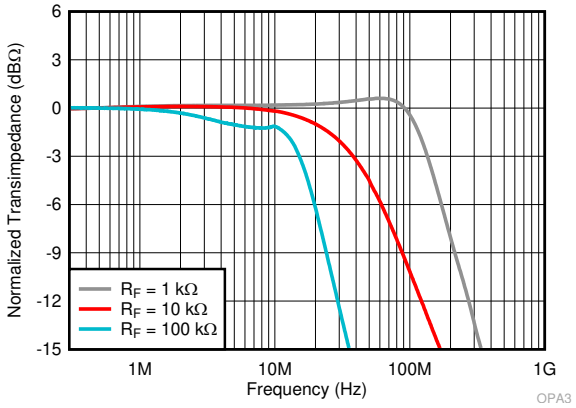
OPA3S2859-EP は、広帯域トランスインピーダンスおよび電圧アンプ・アプリケーション用の、広帯域、低ノイズの CMOS 入力プログラマブル・ゲイン・アンプです。本デバイスをトランスインピーダンス・アンプ (TIA) として構成した場合、0.9GHz のゲイン帯域幅積 (GBWP) により、低容量フォトダイオード (PD) アプリケーションで高い閉ループ帯域幅を実現できます。

3 つの内部スイッチ付き帰還パスを利用し、スイッチなしの 1 つの並列帰還パスを任意で併用することで、最大 4 つのゲイン構成を選択できます。スイッチを内蔵することで、ディスクリートの外付けスイッチを使うシステムに比べて、寄生素子による影響を最小限に抑え、性能を向上させることができます。各スイッチは、広ダイナミック・レンジ・アプリケーションに対応して、1kΩ 未満から 100kΩ を上回る範囲の帰還抵抗値に最適化されています。スイッチ・パスの選択は、どちらのチャネルも 2 線式パラレル・インターフェイスを使って制御されます。選択された各チャネルに対して、ラッチ・ピンをアサートすることでゲイン・パスが変わらないようにすることもできます。これにより、選択されたチャネルのスイッチ制御を無効にし、チャネルのゲインが変わらないようにできます。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
OPA3S2859-EP	WQFN (24)	4.00mm × 4.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。



トランスインピーダンス帯域幅と周波数との関係

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4 Revison History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (April 2021) to Revision B (December 2021)	Page
• データシートのステータスを「事前情報」から *「量産データ」に変更*	1

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5 Pin Configuration and Functions

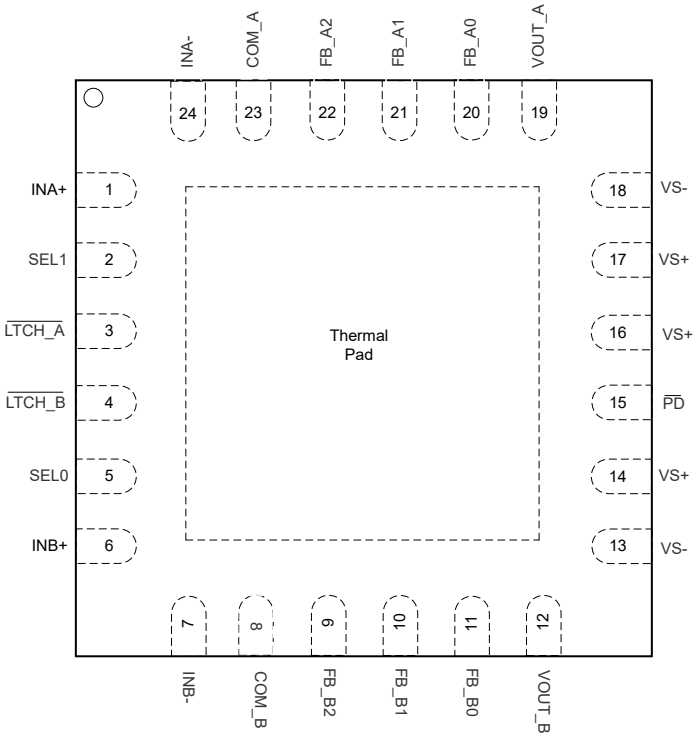

図 5-1. RTW Package
24-Pin WQFN With Exposed Thermal Pad
Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COM_A	23	I	Photodiode input – Channel A
COM_B	8	I	Photodiode input – Channel B
FB_A0	20	I	Feedback connection to Channel A – TIA Gain Resistor (Low gain, optimized for gain in < 10 kΩ range)
FB_A1	21	I	Feedback connection to Channel A – TIA Gain Resistor (Mid gain, optimized for gain in 10 kΩ – 100 kΩ range)
FB_A2	22	I	Feedback connection to Channel A – TIA Gain Resistor (High gain, optimized for gain in > 100 kΩ range)
FB_B0	11	I	Feedback connection to Channel B – TIA Gain Resistor (Low gain, optimized for gain in < 10 kΩ range)
FB_B1	10	I	Feedback connection to Channel B – TIA Gain Resistor (Mid gain, optimized for gain in 10 kΩ – 100 kΩ range)
FB_B2	9	I	Feedback connection to Channel B – TIA Gain Resistor (High gain, optimized for gain in > 100 kΩ range)
INA-	24	I	Negative (inverting) input for amplifier A
INA+	1	I	Positive (noninverting) input for amplifier A
INB-	7	I	Negative (inverting) input for amplifier B
INB+	6	I	Positive (noninverting) input for amplifier B

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表 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{LTCH\_A}}$	3	I	Latch control input for Channel A. $\overline{\text{LTCH\_A}}$ = logic high (default) = transparent mode, gain setting changes based on SEL0 and SEL1 pins are reflected at the output. $\overline{\text{LTCH\_A}}$ = logic low = latch mode = changing SEL0 and SEL1 pins does not affect the gain configuration of amplifier.
$\overline{\text{LTCH\_B}}$	4	I	Latch control input for Channel B. $\overline{\text{LTCH\_B}}$ = logic high (default) = transparent mode, gain setting changes based on SEL0 and SEL1 pins are reflected at the output. $\overline{\text{LTCH\_B}}$ = logic low = latch mode = changing SEL0 and SEL1 pins does not affect the gain configuration of amplifier.
$\overline{\text{PD}}$	15	I	Power down pin. $\overline{\text{PD}}$ = logic high (default) = normal operation, $\overline{\text{PD}}$ = logic low = power down mode.
SEL0	5	I	TIA gain selection. SEL0 = logic high (default). See 表 5-2 for details.
SEL1	2	I	TIA gain selection. SEL1 = logic high (default). See 表 5-2 for details.
VOUT_A	19	O	Output of amplifier A
VOUT_B	12	O	Output of amplifier B
VS-	13, 18	I	Negative (lowest) power supply
VS+	14, 16, 17	I	Positive (highest) power supply
Thermal pad		—	Connect the thermal pad to the most negative power supply (pin 13 and 18) of the device under test (DUT).

表 5-2. Select Pin Decoder

SEL1	SEL0	Gain
LOW	HIGH	Low Gain, optimized for gain in < 10 kΩ range
LOW	LOW	Mid Gain, optimized for gain in 10 kΩ – 100 kΩ range
HIGH	LOW	High Gain, optimized for gain in > 100 kΩ range
HIGH (Default)	HIGH (Default)	External Gain. All internal switches open

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Total supply voltage (V_{S+} - V_{S-})		5.5	V
V_{IN+}, V_{IN-}	Input voltage	(V_{S-}) – 0.5	(V_{S+}) + 0.5	V
V_{ID}	Differential input voltage		1	V
V_{OUT}	Output voltage	(V_{S-}) – 0.5	(V_{S+}) + 0.5	V
I_{IN}	Continuous input current		±4	mA
I_{OUT}	Continuous output current(2)		25	mA
T_J	Junction temperature		150	°C
T_A	Operating free-air temperature	–55	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Long-term continuous output current for electromigration limits

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1500	V
		Charged device model (CDM), per JEDEC specification JEDEC JS-002, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Total supply voltage (V_{S+} - V_{S-})	3.3	5	5.25	V
T_A	Ambient temperature	–55		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA3S2859-EP RTW 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	54.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	30.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	13.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

V_{S+} = 5 V, V_{S-} = 0 V, R_L = 200 Ω, output load is referenced to midsupply, input common-mode biased at midsupply, and T_A ≈ +25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal transimpedance bandwidth(1)	V_{OUT} = 100 mV_{PP}, Gain = 1 kΩ, C_{IN}= 4 pF		130		MHz
		V_{OUT} = 100 mV_{PP}, Gain = 10 kΩ, C_{IN} = 4 pF		40		MHz
		V_{OUT} = 100 mV_{PP}, Gain = 100kΩ, Cin = 4 pF		14		MHz
GBWP	Gain-bandwidth product			900		MHz
	Slew rate (10% - 90%)	V_{OUT} = 2-V step		350		V/µs
e_n	Input-referred voltage noise	f = 1 MHz		2.2		nV/√Hz
Z_{OUT}	Closed-loop output impedance	f = 1 MHz		0.02		Ω
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain	f = DC	70	76		dB
A_{OL}	Open-loop voltage gain	T_A = -55°C to +125°C	64			dB
V_{OS}	Input offset voltage	T_A = -55°C to +125°C	–8	±0.9	8	mV
$\Delta V_{OS}/\Delta T$	Input offset voltage drift	T_A = -55°C to +125°C		–2		µV/°C
I_{BN}, I_{BI}	Input bias current(2)		–50		50	pA
I_{BOS}	Input offset current(2)		-50		50	pA
CMRR	Common-mode rejection ratio	V_{CM} = ±0.5 V (from midsupply), T_A = -55°C to +125°C	67	78		dB
INPUTS						
C_{IN+}	Non-inverting input capacitance			1.4		pF
C_{IN-}	Inverting input capacitance (3)			3		pF
V_{IH}	Common-mode input range (high)	CMRR > 62 dB , T_A = -55°C to +125°C	3.4	3.6		V
V_{IH}	Common-mode input range (high)	CMRR > 62 dB , V_{S+} = 3.3 V, T_A = -55°C to +125°C	1.7	1.9		V
V_{IL}	Common-mode input range (low)	CMRR > 62 dB , T_A = -55°C to +125°C		0	0.4	V
V_{IL}	Common-mode input range (low)	CMRR > 62 dB , V_{S+} = 3.3 V, T_A = -55°C to +125°C		0	0.4	V
OUTPUTS						
V_{OH}	Output voltage (high)	T_A = -55°C to +125°C	3.95	4.1		V
V_{OH}	Output voltage (high)	V_{S+} = 3.3 V, T_A = -55°C to +125°C	2.3	2.4		V
V_{OL}	Output voltage(low)	T_A = -55°C to +125°C		1.1	1.2	V
V_{OL}	Output voltage(low)	V_{S+} = 3.3 V, T_A = -55°C to +125°C		1	1.15	V
I_{O_LIN}	Linear output drive (source and sink)	R_L = 10 Ω, A_{OL} > 52 dB	65	74		mA
I_{O_LIN}	Linear output drive (source and sink)	R_L = 10 Ω, A_{OL} > 52 dB, T_A = -55°C to +125°C	58			mA
CHANNEL-TO-CHANNEL MATCHING						
	Crosstalk (output-referred)	f = 1 MHz, Gain = 100 kΩ, V_{OUT} = 100 mV_{PP}		-70		dB
	Offset voltage mismatch	T_A = -55°C to +125°C	-10		10	mV
	Offset current mismatch		-20		20	pA

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6.5 Electrical Characteristics (continued)

V_{S+} = 5 V, V_{S-} = 0 V, R_L = 200 Ω, output load is referenced to midsupply, input common-mode biased at midsupply, and T_A ≈ +25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_Q	Quiescent current (both channels)	V_{S+} = 5 V		44	53	mA
		V_{S+} = 5 V, T_A = +125°C		51	63	mA
		V_{S+} = 5 V, T_A = -55°C		39	47	mA
PSRR+	Power Supply Rejection Ratio	T_A = -55°C to +125°C	72	85		dB
PSRR-	Power Supply Rejection Ratio	T_A = -55°C to +125°C	66	72		dB
POWER DOWN						
	Disable voltage threshold	Voltage referenced to V_{S+}, amplifier OFF below this voltage, T_A = -55°C to +125°C	V_{S+} - 1.5	V_{S+} - 1.3		V
	Enable voltage threshold	Voltage referenced to V_{S+}, amplifier ON above this voltage, T_A = -55°C to +125°C		V_{S+} - 1.2	V_{S+} - 0.8	V
	Power-down quiescent current			75	140	µA
	Power-down quiescent current	T_A = -55°C to +125°C			170	µA
	$\overline{PD}$ bias current	$V_{\overline{PD}}$ = V_{S-} or V_{S+}		6		µA
	$\overline{PD}$ bias current	$V_{\overline{PD}}$ = V_{S-} or V_{S+} , T_A = -55°C to +125°C			22	µA
	$\overline{PD}$ bias current	$V_{\overline{PD}}$ at switching threshold		160		µA
	$\overline{PD}$ bias current	$V_{\overline{PD}}$ at switching threshold, T_A = -55°C to +125°C			405	µA
	Turnon time delay	Time to V_{OUT} = 90% of final value		90		ns
	Turnoff time delay	Time to V_{OUT} = 10% of final value		330		ns

(1) C_{IN} = Photodiode capacitance + PCB capacitance. Photodiode capacitance is 3.3 pF and estimated PCB capacitance is 0.7 pF.
(2) Leakage currents from switches are not included in this measurement.
(3) C_{IN-} refers to the capacitance at the inverting input of the amplifier. C_{IN-} = $C_{IN-(CM)}$ + C_{DIFF} + Switch capacitance on the amplifier inverting pin (ON capacitance of the closed switch + OFF capacitance for open switches).

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6.6 Switching Characteristics

V_{S+} = 5 V, V_{S-} = 0 V, input common-mode biased at midsupply, R_{F0} = 1 kΩ, R_{F1} = 10 kΩ, R_{F2} = 100 kΩ, R_L = 200 Ω, output load is referenced to midsupply, and T_A ≈ +25°C (unless otherwise noted), see figure 7-1 for schematic configuration. (1) (2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GAIN SWITCHES						
	Switch transition-time (5)	SW_0 OFF to SW_1 ON		160		ns
		SW_0 OFF to SW_2 ON		230		
		SW_1 OFF to SW_0 ON		80		
		SW_1 OFF to SW_2 ON		230		
		SW_2 OFF to SW_0 ON		80		
		SW_2 OFF to SW_1 ON		110		
C_{COM0}	COM capacitance (3) (6)	SW_{COM0} ON; SW_{COM1} and SW_{COM2} OFF		1.3		pF
C_{COM1}		SW_{COM1} ON; SW_{COM0} and SW_{COM2} OFF		1.2		
C_{COM2}		SW_{COM2} ON; SW_{COM0} and SW_{COM1} OFF		1.2		
C_{COM_OPEN}		SW_{COM0} , SW_{COM1} and SW_{COM2} OFF		1.2		
C_{FB0}	FB capacitance (5) (7)	SW_0 ON		1.9		
C_{FB1}		SW_1 ON		1.6		
C_{FB2}		SW_2 ON		1.5		
C_{FB0_OPEN}		SW_0 OFF		1.4		
C_{FB1_OPEN}		SW_1 OFF		1.2		
C_{FB2_OPEN}		SW_2 OFF		1.1		
R_{ON_COM0}	On resistance (8) (9)			80		Ω
R_{ON_FB0}				38		
R_{ON_COM1}				125		
R_{ON_FB1}				37		
R_{ON_COM2}				375		
R_{ON_FB2}				35		
	On resistance channel-to-channel matching (3) (4)	SW_{COM0} for Channel A and B		0.15		Ω
		SW_{FB0} for Channel A and B		0.4		
		SW_{COM1} for Channel A and B		0.45		
		SW_{FB1} for Channel A and B		0.07		
		SW_{COM2} for Channel A and B		3		
		SW_{FB2} for Channel A and B		0.12		

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6.6 Switching Characteristics (continued)

V_{S+} = 5 V, V_{S-} = 0 V, input common-mode biased at midsupply, R_{F0} = 1 kΩ, R_{F1} = 10 kΩ, R_{F2} = 100 kΩ, R_L = 200 Ω, output load is referenced to midsupply, and T_A ≈ +25°C (unless otherwise noted), see figure 7-1 for schematic configuration. (1) (2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC PIN FUNCTION (LATCH, SEL)						
	Logic low threshold	Logic low below the threshold voltage, T_A = -55°C to +125°C	V_{S+} - 1.5	V_{S+} - 1.3		V
	Logic high threshold	Logic high above the threshold voltage, T_A = -55°C to +125°C		V_{S+} - 1.2	V_{S+} - 0.8	V
	Bias current	V_{PIN} = V_{S-} or V_{S+}		6		µA
	Bias current	V_{PIN} = V_{S-} or V_{S+} , T_A = -55°C to +125°C			22	µA
	Bias current	V_{PIN} at switching threshold		160		µA
	Bias current	V_{PIN} at switching threshold, T_A = -55°C to +125°C			405	µA
	Setup time		100			ns
	Hold time		100			ns

(1) All the specifications apply for both Channels A and B, unless otherwise noted.
(2) When switching from one gain condition to another, the new gain switches are closed before opening the previous gain switches (make-before-break).
(3) SW_{COM0}, SW_{COM1}, SW_{COM2} refer to switch on the common-mode side (COM) for the different gain options.
(4) SW_{FB0}, SW_{FB1}, SW_{FB2} refer to switch on the feedback side (FB) for the different gain options.
(5) SW_0, SW_1, SW_2 refers to the two switches needed for a given gain condition. For example, SW0 refers to SW_{COM0} and SW_{FB0}.
(6) C_{COM0}, C_{COM1}, C_{COM2} is the capacitance at the COM pin for different gain options. It is equal to ON capacitance of closed switch + OFF capacitance of open switches.
(7) C_{FB0}, C_{FB1}, C_{FB2} is the capacitance at the FB_X pin. It is equal to ON capacitance of the gain option selected (SW_{COM0} + SW_{FB0} capacitance).
(8) R_{ON_COM0}, R_{ON_COM1}, R_{ON_COM2}, refer to ON resistance for the COM side switch.
(9) R_{ON_FB0}, R_{ON_FB1}, R_{ON_FB2}, refer to ON resistance for the FB side switch.

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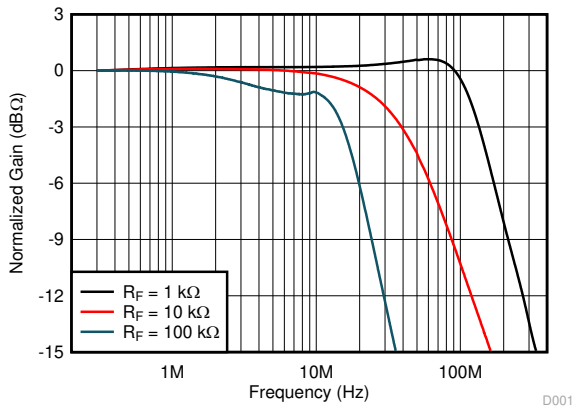
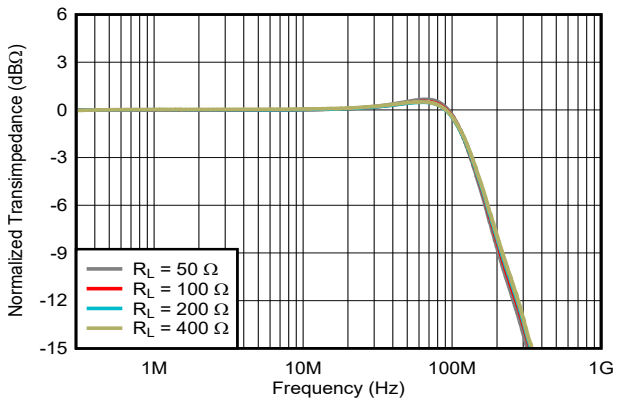
6.7 Typical Characteristics

V_{S+} = +2.5 V, V_{S-} = -2.5 V, R_L = 200 Ω, C_{IN} = 4 pF, output load is referenced to mid-supply, input common-mode biased at mid-supply, and T_A ≈ +25°C (unless otherwise noted)



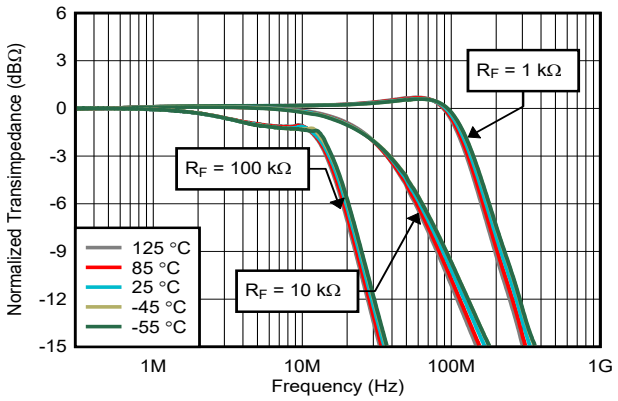
V_{OUT} = 100 mV_{PP}

図 6-1. Small-Signal Frequency Response vs Gain



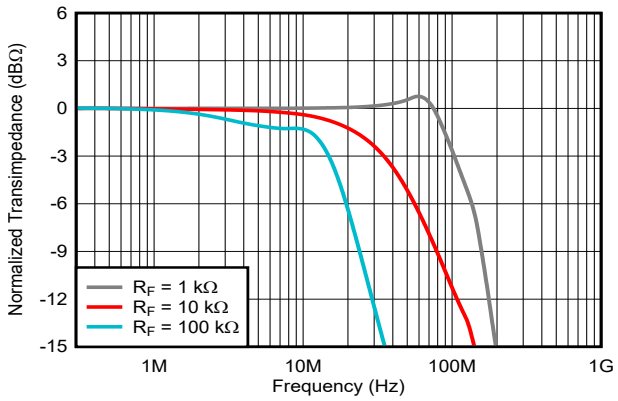
V_{OUT} = 100 mV_{PP}, R_F = 1 kΩ

図 6-2. Small-Signal Frequency Response vs Output Load



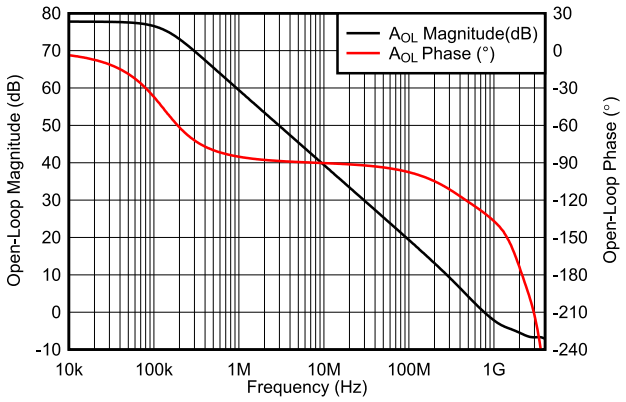
V_{OUT} = 100 mV_{PP}

図 6-3. Small-Singal Frequency Response vs Ambient Temperature



V_{OUT} = 2 V_{PP}

図 6-4. Large-Signal Frequency Response vs Gain



V_{OUT} = 100 mV_{PP}

図 6-5. Open-Loop Magnitude and Phase vs Frequency

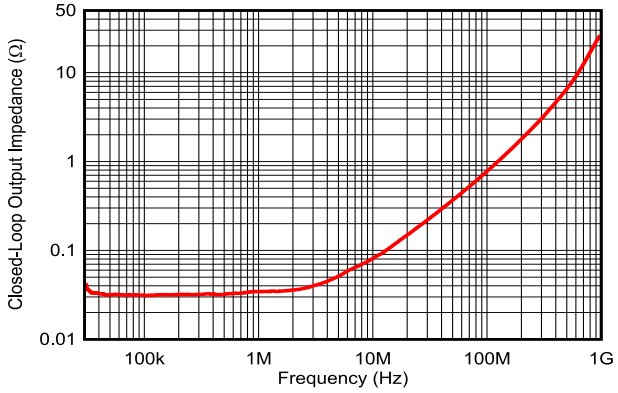


図 6-6. Closed-Loop Output Impedance vs Frequency

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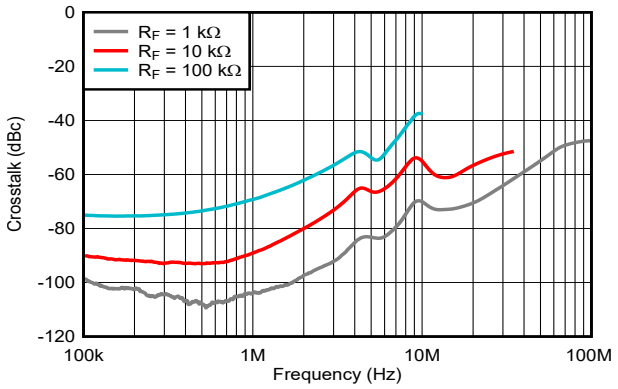
6.7 Typical Characteristics (continued)

V_{S+} = +2.5 V, V_{S-} = -2.5 V, R_L = 200 Ω, C_{IN} = 4 pF, output load is referenced to mid-supply, input common-mode biased at mid-supply, and T_A ≈ +25°C (unless otherwise noted)



V_{OUT} = 2 V_{PP}

図 6-7. Large-Signal Crosstalk vs Gain

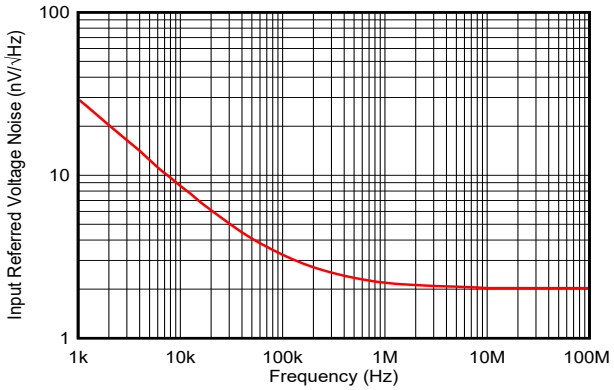


図 6-8. Voltage Noise Density vs Frequency

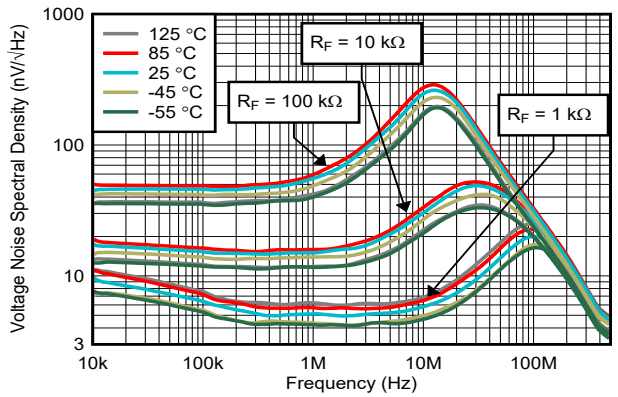
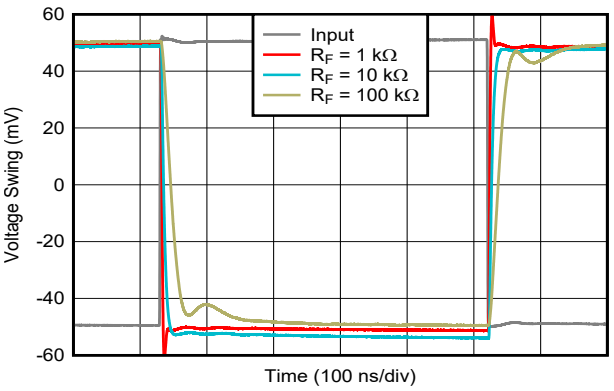
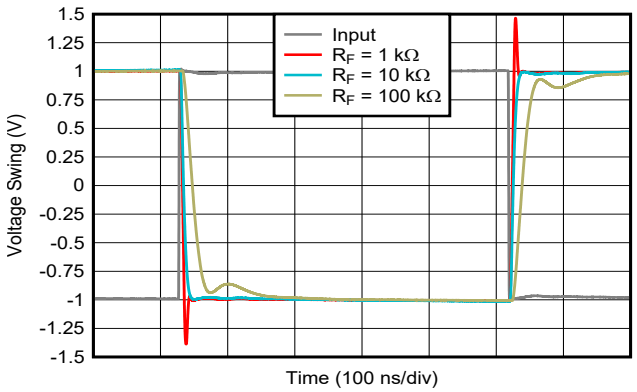


図 6-9. Voltage Noise Density vs Ambient Temperature



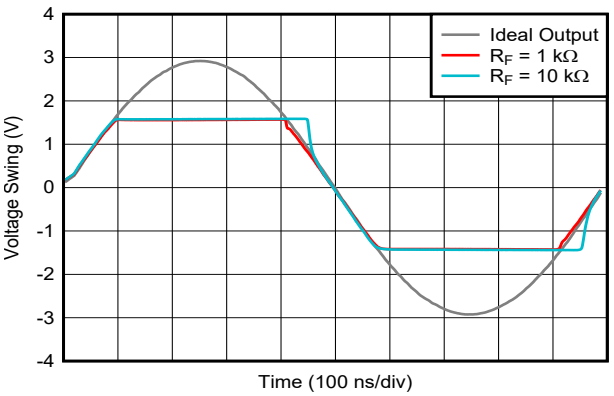
V_{OUT} = 100 mV_{PP}

図 6-10. Small-Signal Transient Response



V_{OUT} = 2 V_{PP}

図 6-11. Large-Signal Transient Response



2X Output Overdrive

図 6-12. Output Overload Reponse − Low Gain Settings

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6.7 Typical Characteristics (continued)

V_{S+} = +2.5 V, V_{S-} = -2.5 V, R_L = 200 Ω, C_{IN} = 4 pF, output load is referenced to mid-supply, input common-mode biased at mid-supply, and T_A ≈ +25°C (unless otherwise noted)

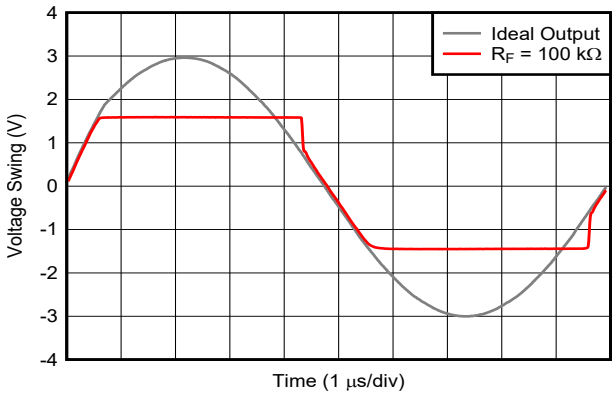

図 6-13. Output Overload Reponse − High Gain Setting

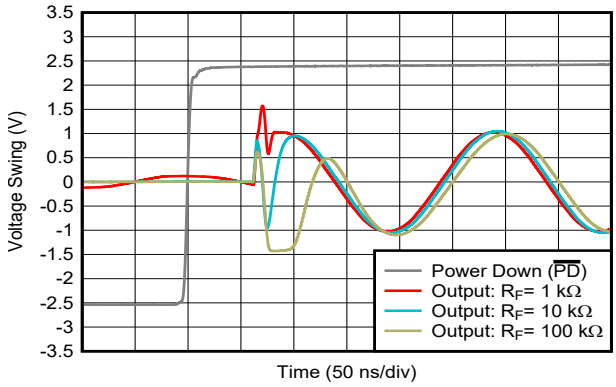

図 6-14. Turn-On Transient Response

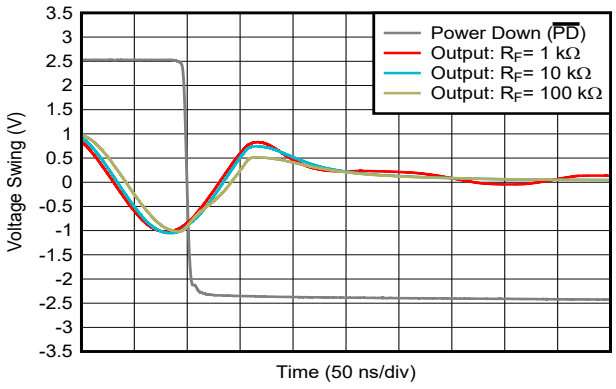

図 6-15. Turn-Off Transient Response

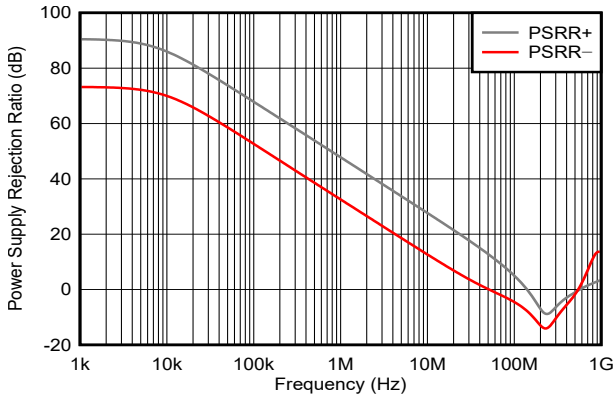

図 6-16. Power Supply Rejection Ratio vs Frequency

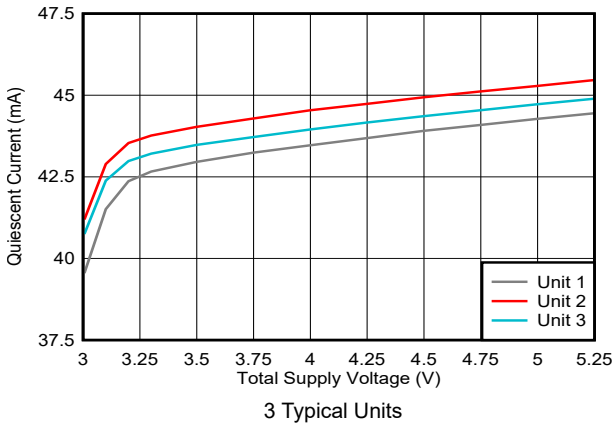

図 6-17. Quiescent Current (Both Channels) vs Supply Voltage

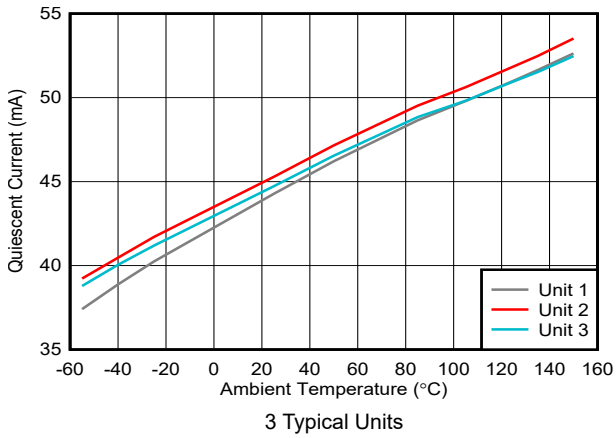

図 6-18. Quiescent Current (Both Channels) vs Ambient Temperature

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6.7 Typical Characteristics (continued)

V_{S+} = +2.5 V, V_{S-} = -2.5 V, R_L = 200 Ω, C_{IN} = 4 pF, output load is referenced to mid-supply, input common-mode biased at mid-supply, and T_A ≈ +25°C (unless otherwise noted)

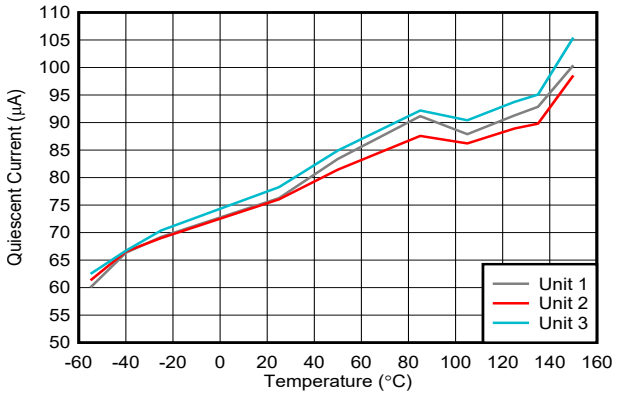

図 6-19. Quiescent Current (Amplifiers Disabled) vs Ambient Temperature

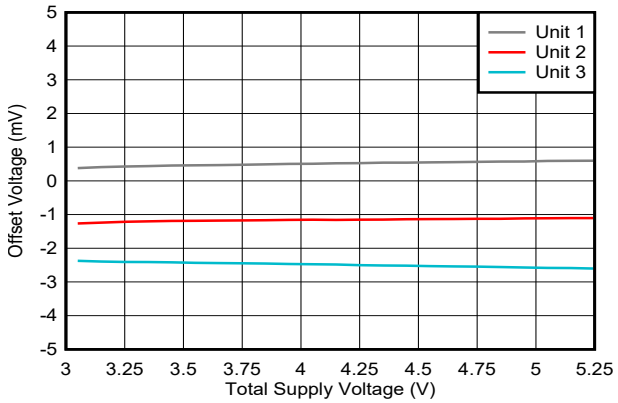

図 6-20. Offset Voltage vs Supply Voltage

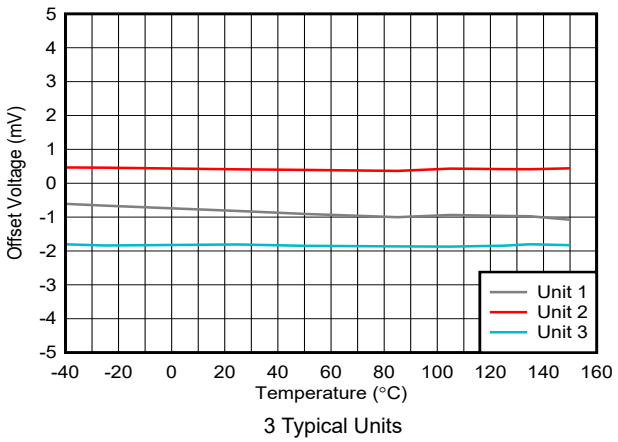

図 6-21. Offset Voltage vs Ambient Temperature

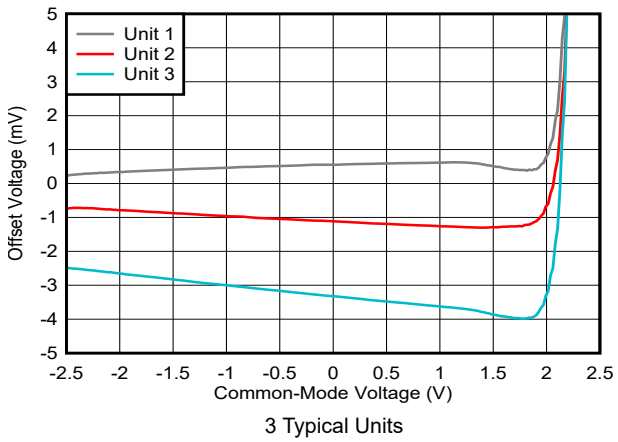

図 6-22. Offset Voltage vs Input Common-Mode Voltage

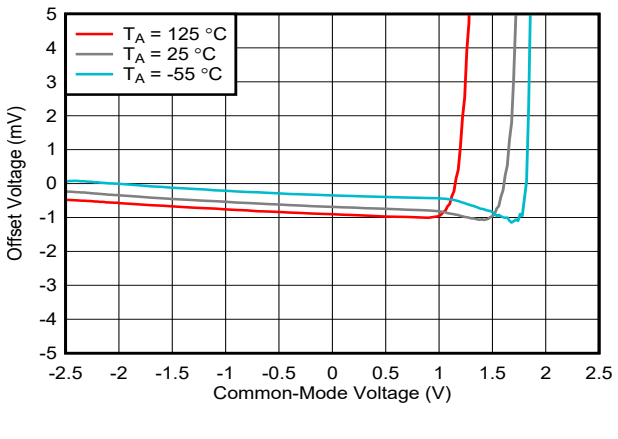

図 6-23. Offset Voltage vs Input Common-Mode Voltage vs Ambient Temperature

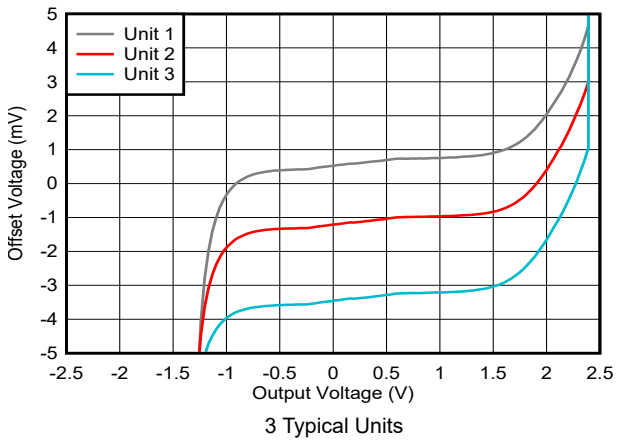

図 6-24. Offset Voltage vs Output Swing

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6.7 Typical Characteristics (continued)

V_{S+} = +2.5 V, V_{S-} = -2.5 V, R_L = 200 Ω, C_{IN} = 4 pF, output load is referenced to mid-supply, input common-mode biased at mid-supply, and T_A ≈ +25°C (unless otherwise noted)

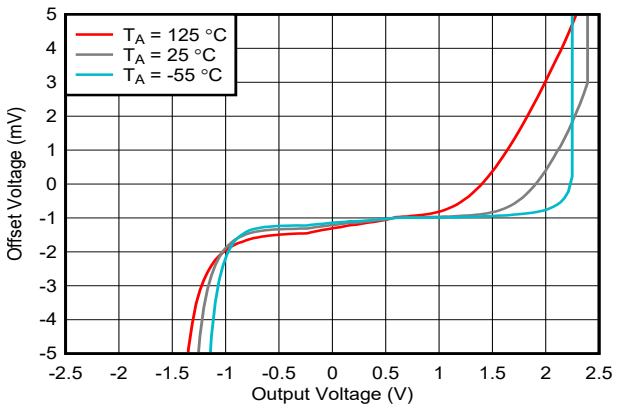
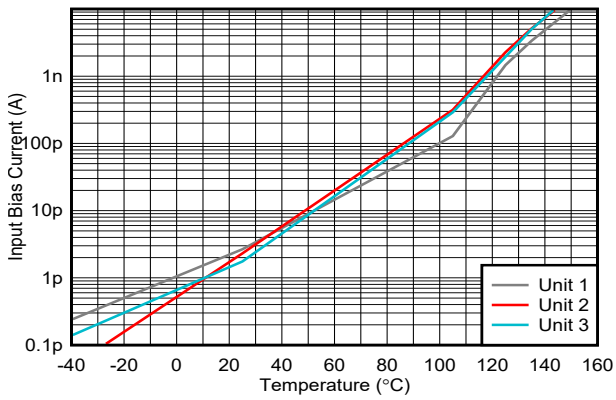
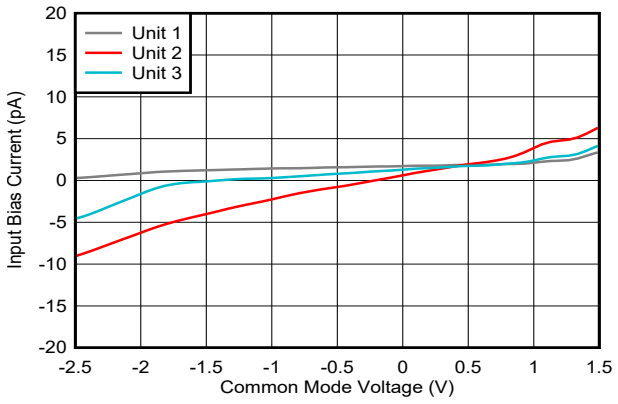


図 6-25. Offset Voltage vs Output Swing vs Ambient Temperature



3 Typical Units

図 6-26. Input Bias Current vs Ambient Temperature



3 Typical Units

図 6-27. Input Bias Current vs Input Common-Mode Voltage

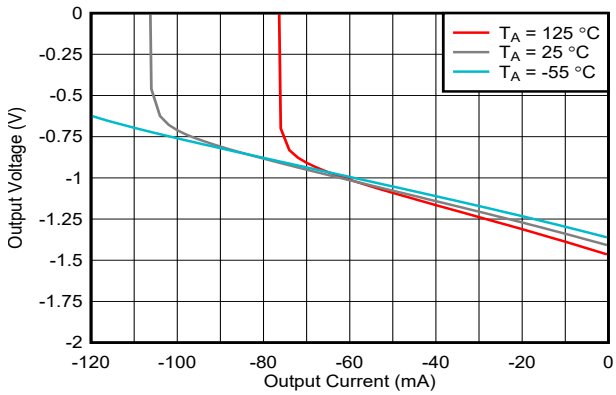


図 6-28. Output Swing vs Sinking Current

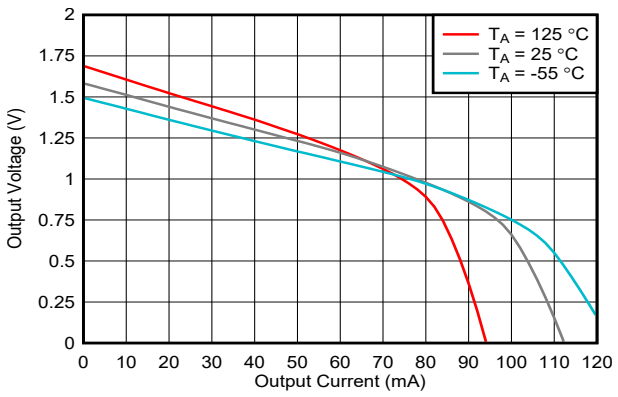
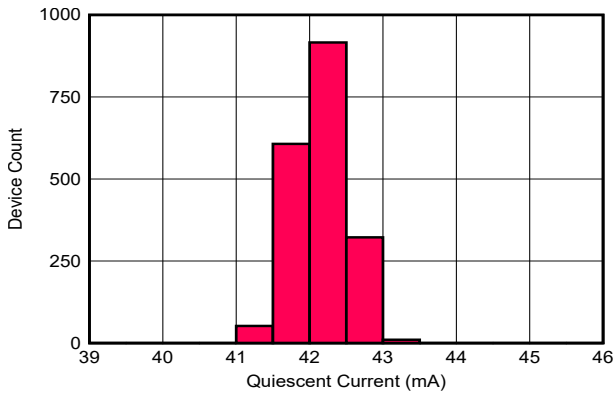


図 6-29. Output Swing vs Sourcing Current



μ = 42.2 mA, σ = 0.251 mA

図 6-30. Quiescent Current (Both Channels) Distribution

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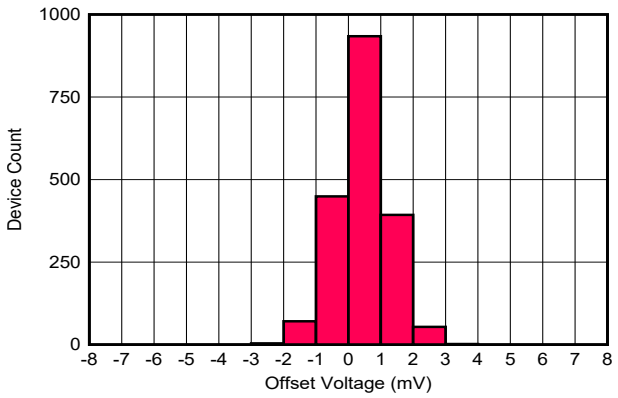
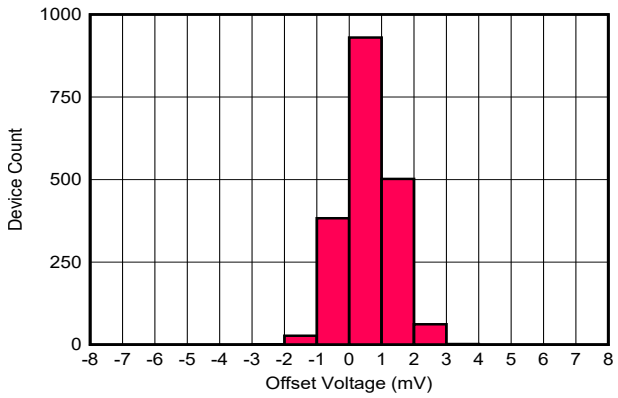
6.7 Typical Characteristics (continued)

V_{S+} = +2.5 V, V_{S-} = -2.5 V, R_L = 200 Ω, C_{IN} = 4 pF, output load is referenced to mid-supply, input common-mode biased at mid-supply, and T_A ≈ +25°C (unless otherwise noted)



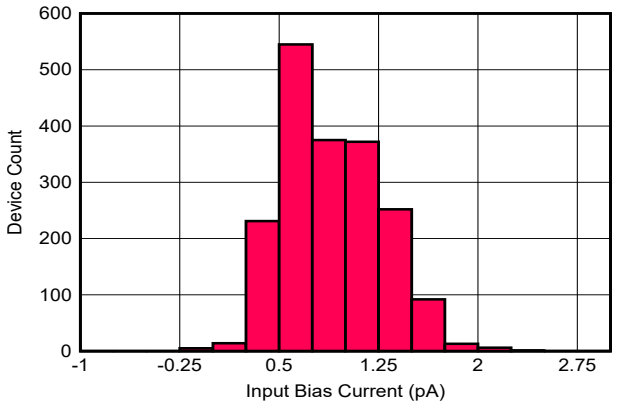
μ = 0.450 mV, σ = 0.845 mV

図 6-31. Offset Voltage Distribution − Channel A



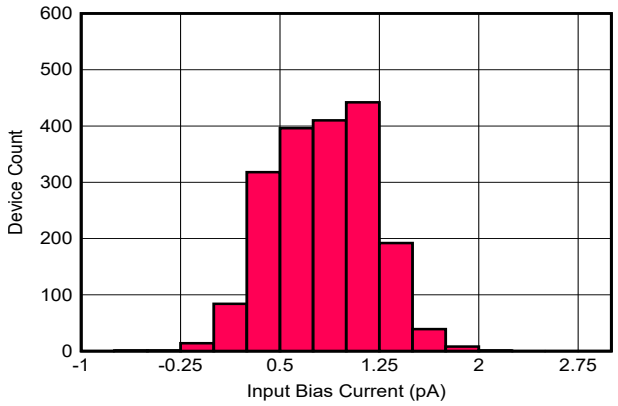
μ = 0.606 mV, σ = 0.754 mV

図 6-32. Offset Voltage Distribution − Channel B



μ = 0.896 pA, σ = 0.383 pA

図 6-33. Input Bias Current Distribution − Channel A



μ = 0.825 pA, σ = 0.386 pA

図 6-34. Input Bias Current Distribution − Channel B

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7 Parameter Measurement Information

The test setup configuration for OPA3S2859-EP is shown below.

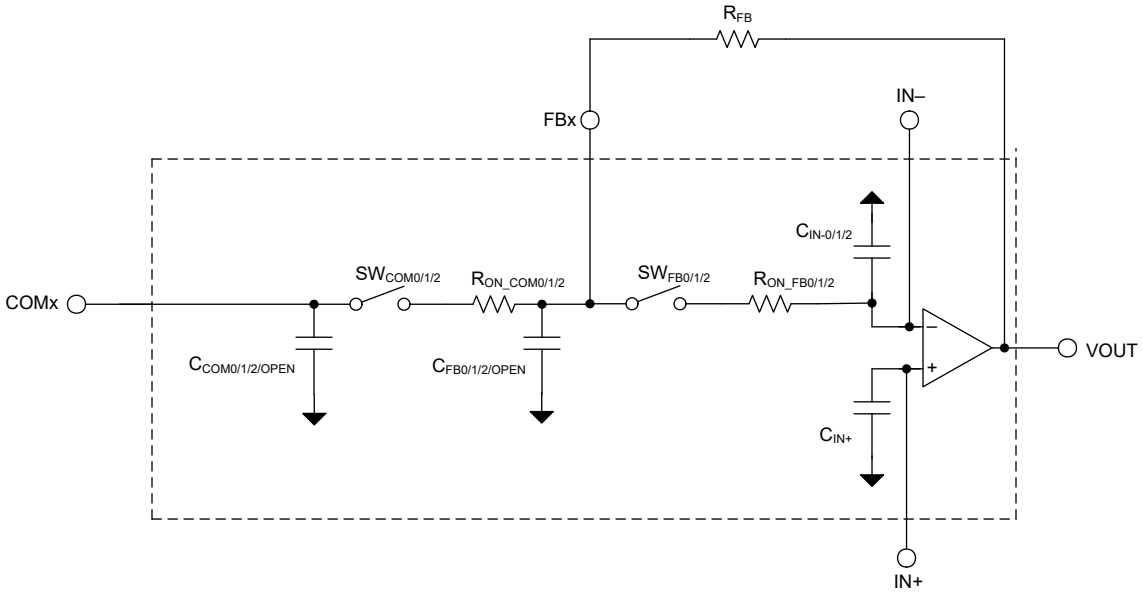

図 7-1. Switching Characteristics Configuration

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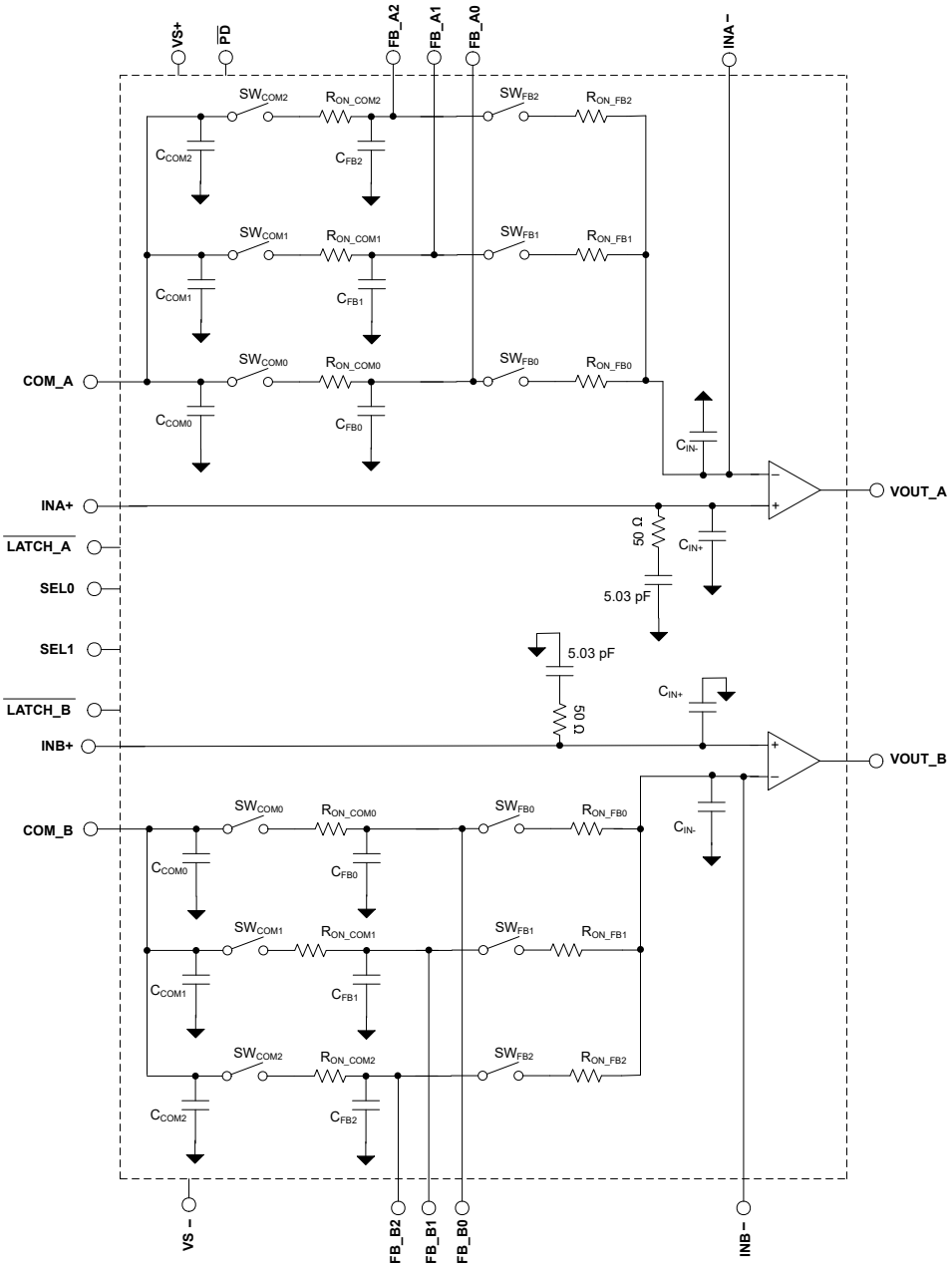
8 Detailed Description

8.1 Overview

The OPA3S2859-EP features dual channel, high-speed, low noise, wide gain bandwidth amplifier with programmable gain switches to offer a compact, easy-to-use device for wideband transimpedance applications, high-speed data acquisition systems, and applications with weak signal inputs that require low-noise and high-gain front ends. Integrated switches allow for multiple gain settings on a single amplifier stage without the need for an additional multiplexer, therefore minimizing board parasitics.

The OPA3S2859-EP is offered in a 4-mm × 4-mm, 24-pin WQFN package that features multiple feedback (FB) pins for different gain options to make simple feedback network connection between the amplifier output and inverting input. The three internally switched feedback paths along with an additional parallel non-switched feedback path allows for up to four selectable gain configurations.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Programmable Gain

The OPA3S2859-EP features integrated switches that can be used for implementing different gain configurations. The closed-loop bandwidth and noise of a TIA are affected by the transimpedance gain and photodiode capacitance. The OPA3S2859-EP has a higher bandwidth in its low-gain configuration for a given value of photodiode capacitance compared to the high-gain configuration. Increasing the gain of the TIA stage by a factor of *X* increases the output signal by a factor *X*, but the noise contribution from the resistor only increases by √X. The input-referred noise density of the low-gain configuration is therefore higher than the input-referred noise density of the high-gain configuration.

OPA3S2859-EP provides control for switching among three independently-configured external feedback networks using FB_x0, FB_x1, FB_x2 pins, and allows for up to four selectable gain configurations with an additional parallel non-switched feedback path. The internal switches minimize parasitic contributions to increase performance compared to external methods. Each switch is optimized for increasing feedback resistor values ranging from < 1 kΩ to > 100 kΩ for wide dynamic range applications. The selected switch path is controlled for both channels using a 2-wire parallel interface (SEL0 and SEL1).

In many systems it is typical that gain will switch sequentially (also known as adjacent gain switching). For example, the gain will switch low to medium to high or high to medium to low. When switching between adjacent gains, the switches feature make-before-break switching, when programmed to a different switch connection, the previous switch does not change to high impedance state until the new switch is closed, with a typical 80 ns to 230 ns delay when both switches are closed. This feature helps the amplifier from not operating in an open-loop state when the switches are used in a switched-gain transimpedance configuration.

8.3.2 Slew Rate

The OPA3S2859-EP features a high slew rate of 350 V/µs. The slew rate is a critical parameter in high-speed pulse applications such as optical time-domain reflectometry (OTDR). The high slew rate implies that the device accurately reproduces a 2-V, sub 100-ns pulse edge, as seen in 図 6-11. The wide bandwidth and slew rate of the device make it an excellent amplifier for high-speed signal-chain front ends.

8.3.3 Input and ESD Protection

The OPA3S2859-EP is fabricated on a low-voltage, high-speed, BiCMOS process. The internal, junction breakdown voltages are low for these small geometry devices, and as a result, all device pins are protected with internal ESD protection diodes to the power supplies. There are two antiparallel diodes between the inputs of the amplifier that clamp the inputs during an overrange or fault condition.

8.4 Device Functional Modes

8.4.1 Split-Supply and Single-Supply Operation

The OPA3S2859-EP can be configured with single-sided supplies or split-supplies without degrading performance. In either case, the thermal pad should be tied to the same voltage as V_{S-}.

8.4.2 Power-Down Mode

The OPA3S2859-EP features a power-down mode to conserve power. Connecting the $\overline{PD}$ pin low disables the amplifier thereby reducing the quiescent current and places the output in a high-impedance state.

$\overline{PD}$ pin has an internal pull up resistor, if the pin is left floating then the device defaults to an ON state. The $\overline{PD}$ disable and enable threshold voltages are with reference to the positive supply, as shown in the *Electrical Characteristics* section. If the amplifier is configured with the positive supply at 5 V and the negative supply at ground, then the disable and enable threshold voltages are 3.5 V and 4.2 V, respectively. If the amplifier is configured with ±2.5 V supplies, then the threshold voltages are at 1 V and 1.7 V.

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8.4.3 Gain Select Mode (SEL)

The OPA3S2859-EP features two pins SEL0 and SEL1 to choose between three different internal switch networks and an external option. The SELx disable and enable threshold voltages are with reference to the positive supply as shown in the *Switching Characteristics* table. Note: while the SELx logic will select the same switch configuration for channel A and B, the external components (feedback network) of channels A and B do not have to be exactly the same.

When switching between different gain settings (feedback networks), the device has a transition time of only 80 ns to 230 ns (typical) as shown in the *Switching Characteristics* table. In many systems, it is typical that gain will be stepped sequentially (for example, low to medium to high or high to medium to low). The SELx logic assignment ensures that switching gains up or down involve only one input-pin transition, reducing the probability of unintended false codes during logic settling, as shown in 表 5-2.

8.4.4 Latch Mode

OPA3S2859-EP features $\overline{\text{LTCH\_A}}$ and $\overline{\text{LTCH\_B}}$ pins which independently latch the gain configuration for Channel A and Channel B, respectively. If the latch control inputs are connected to logic high or floating, then the chosen feedback selection (through the SEL0 and SEL1 pins) applies to A and B analog channels immediately, this is also called transparent mode. If the latch control inputs are logic low, then changing the feedback selection (through the SEL0 and SEL1 pins) does not affect the gain configuration of the respective amplifier channel. 図 8-1 shows minimum timing requirements that should be met when using $\overline{\text{LTCH\_x}}$ pins to latch gain configuration.

By using the latch control input for each channel, the feedback selection can be controlled separately from the common SEL1 and SEL0 pins, see an example below. The latch control inputs can also provide benefits in some cases where channel A and B need to have the same configuration. For example, in transparent mode, when switching between different gain settings any timing skew from SEL1 and SEL0 may result in unintended switch logic configurations for a short-duration resulting in transient output glitch. These intermediate glitch states can be minimized by holding the $\overline{\text{LTCH\_x}}$ pin low until the new selection value at SEL pins has settled.

This feature is also useful in larger systems with multiple OPA3S2859-EP devices, the gain path can be set using common SEL0 and SEL1 signals for all the devices and latch pins can be used to control the gain independently for each amplifier channel.

Example configuration, to update the gain settings for Channel A only, follow these steps:

1. Set $\overline{\text{LTCH\_B}}$ to logic low (latch mode), this way changes made on Channel A do not affect Channel B gain configuration.

2. If $\overline{\text{LTCH\_A}}$ is high (transparent mode), use SEL0 and SEL1 pins to select the feedback network of interest. If $\overline{\text{LTCH\_A}}$ is low, toggle it to logic high and use SEL0 and SEL1 pins to select the feedback network of interest.

3. To hold the selected gain, set $\overline{\text{LTCH\_A}}$ to logic low. Ensure minimum setup time requirements (100 ns) are met between SELx selection to $\overline{\text{LTCH\_A}}$ going low. Also, ensure that during the hold time (100 ns), no changes should be made on SELx pins. The minimum timing is based on internal device configuration, if needed, additional time must be added due to board layout parasitics and signal delays.

4. Gain setting for channel A is now latched and any changes on SELx pins will not change the gain configuration for channel A.

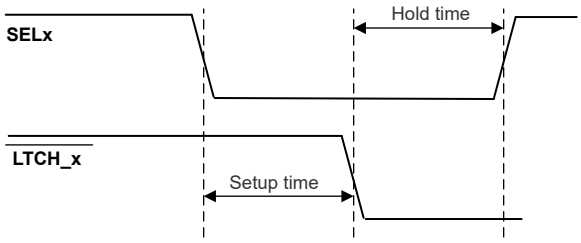

図 8-1. Timing Diagram

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The OPA3S2859-EP offers a unique combination of dual channel, wide bandwidth low noise amplifiers with integrated programmable gain switches. This combination makes this amplifier an excellent choice for photodiode transimpedance amplifier applications with variable gain needs.

9.2 Typical Application

図 9-1 shows the circuit used to measure transimpedance bandwidth of the OPA3S2859-EP with different feedback network setting options. This configuration imitates the impedance of the photodiode on the input of the TIA.

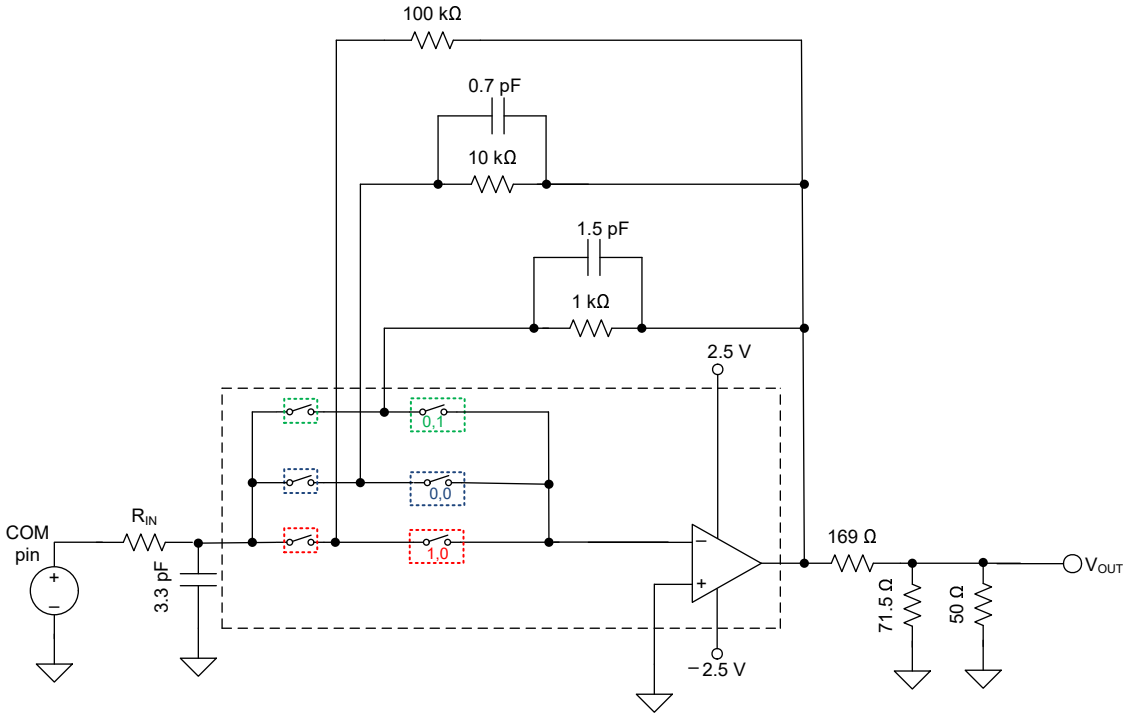

図 9-1. OPA3S2859-EP Test Circuit

9.2.1 Design Requirements

The objective is to design a variable gain, low noise, wideband optical front-end transimpedance amplifier. The design requirements are:

- Amplifier supply voltage: ± 2.5 V
- Transimpedance gain: 1 kΩ, 10 kΩ, 100 kΩ
- Photodiode capacitance: C_{APD} = 3.3 pF (additional estimated PCB capacitance = 0.7 pF)
- Target bandwidth: 130 MHz, 40 MHz, 14 MHz

9.2.2 Detailed Design Procedure

The OPA3S2859-EP meets the growing demand for wideband, low-noise photodiode amplifiers. The closed-loop bandwidth of a transimpedance amplifier is a function of the following:

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1. The total input capacitance (C_{IN}). This total includes the photodiode capacitance, the input capacitance of the amplifier (common-mode and differential capacitance) and any stray capacitance from the PCB.
2. The op amp gain bandwidth product (GBWP).
3. The transimpedance gain (R_F).

図 9-1 shows the OPA3S2859-EP configured as programmable gain TIA using different feedback paths through the switch network. The feedback resistance (R_F) and the input capacitance (C_{IN}) form a zero in the noise gain that results in instability if left unchecked. To counteract the effect of the zero, a pole is inserted into the noise gain transfer function by adding the feedback capacitor (C_F). The *Transimpedance Considerations for High-Speed Amplifiers Application Report* discusses theories and equations that show how to compensate a transimpedance amplifier for a particular transimpedance gain and input capacitance. The bandwidth and compensation equations from the application report are available in an Excel® calculator. *What You Need To Know About Transimpedance Amplifiers – Part 1* provides a link to the calculator.

The equations and calculators in the referenced application report and blog posts are used to model the bandwidth (f_{-3dB}) and noise performance of the OPA3S2859-EP configured as a TIA. For this setup, to emulate an ideal current source, choose R_{IN} value to be 1 to 10x greater than R_F such that the low frequency noise gain closer to 1 V/V to 2 V/V (R_F = 1 kΩ, 10 kΩ, 100 kΩ, R_{IN} = 10 kΩ, 100 kΩ, 100 kΩ; respectively). The resultant performance is shown in 図 9-2. To maximize bandwidth, make sure to reduce any stray parasitic capacitance from the PCB. Increasing R_F results in lower bandwidth. To maximize the signal-to-noise ratio (SNR) in an optical front-end system, maximize the gain in the TIA stage.

9.2.3 Application Curves

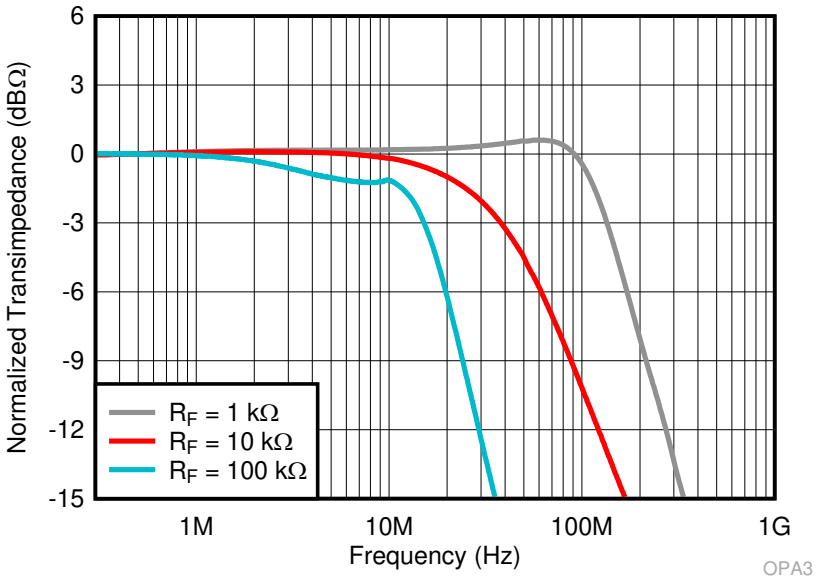

図 9-2. Bandwidth vs Frequency

10 Power Supply Recommendations

The OPA3S2859-EP operates on supplies from 3.3 V to 5.25 V. The device operates on single-sided supplies, split and balanced bipolar supplies, and unbalanced bipolar supplies. Because the OPA3S2859-EP does not feature rail-to-rail inputs or outputs, the input common-mode and output swing ranges are limited at 3.3-V supplies.

11 Layout

11.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier, such as the OPA3S2859-EP, requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include the following:

- **Reduce capacitive coupling between feedback traces.** Trace-to-trace capacitance between the three feedback connection traces can cause the traces to couple together at high frequency and effect the gain of the device. Particularly for high gain feedback configurations, capacitive coupling to feedback paths with lower gain can significantly reduce the bandwidth if not properly isolated. For example, in a circuit configuration with 100k, 10k, and 1k feedback elements, the 100k gain path can see over 66% reduction in bandwidth when using an non-optimized feedback layout. To properly isolate the feedback traces it is important to space the traces out and pour ground plane between the traces to isolate their capcitance; additional trace length, however, does add further inductance and capacitance to the traces which can also effect performance. Therefore, it is important to balance the feedback area and trace length to best minimize the major parasitic effect. A good starting point is to use a design similar to the evaluation module with a feedback area of approximately 6 mm × 6 mm. This can then be adjusted depending on circuit limitations and needs.
- **Minimize parasitic capacitance from the signal I/O pins to ac ground.** Parasitic capacitance on the output pins can cause instability where as parasitic capacitance on the input pin reduces the amplifier bandwidth. To reduce unwanted capacitance, cut out the power and ground traces under the signal input pins, output pins, and exterior feedback trace when possible. A small value isolation resistor between the DUT output and feedback network can also help reduce the parasitic loading caused by the feedback trace on the output. Otherwise, ground and power planes must be unbroken elsewhere on the board.
- **Minimize the distance from the power-supply pins to the high-frequency bypass capacitors.** Use high-quality, 100-pF to 0.1-µF, C0G and NPO-type decoupling capacitors with voltage ratings at least three times greater than the amplifiers maximum power supplies. Place the smallest value capacitors on the same side as the DUT. If space constraints force the larger value bypass capacitors to be placed on the opposite side of the PCB, use multiple vias on the supply and ground side of the capacitors. This configuration makes sure that there is a low-impedance path to the amplifiers power-supply pins across the amplifiers gain bandwidth specification. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Larger (2.2-µF to 6.8-µF) decoupling capacitors that are effective at lower frequency must be used on the supply pins. Place these decoupling capacitors further from the device. Share the decoupling capacitors among several devices in the same area of the printed circuit board (PCB).

11.2 Layout Examples

図 11-1 shows a typical layout around the OPA3S2859-EP based on the evaluation module. The smallest decoupling capacitors were placed as close as possible to the DUT with wide metal area to minimize inductance. Special attention was placed on the feedback network layout to optimize the design for a typical application using 1 kΩ, 10 kΩ, and 100 kΩ feedback resistors. Please see 図 11-2 for more details. The black colored areas under the input and feedback traces show the voids cut in the ground plane underneath the traces to minimize capacitance to ground as much as possible.

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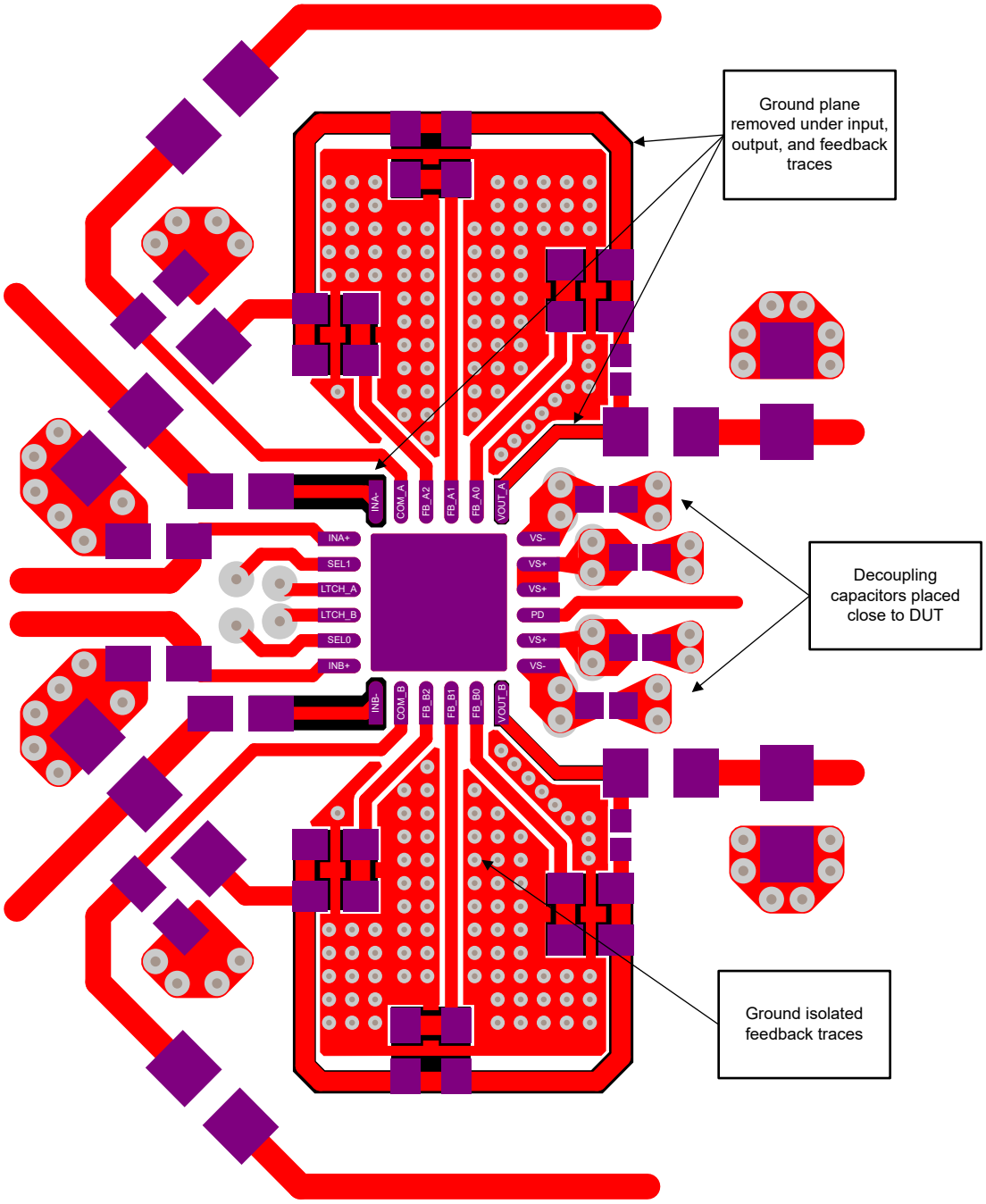

図 11-1. General Layout Example

図 11-2 shows an example of a feedback network from the evaluation module optimized to reduce the capacitive coupling between the feedback and output traces. Ground plane is poured between each of the feedback traces and component footprints as much as possible for the best isolation. A small isoation resistor (RISO) in connected between the output and feedback trace to help isolate the trace capacitance from being directly connected to the DUT output. Additionally, the ground plane is removed from under the feedback trace to further reduce the parasitic capacitance to ground created by the additional trace length required for the feedback network.

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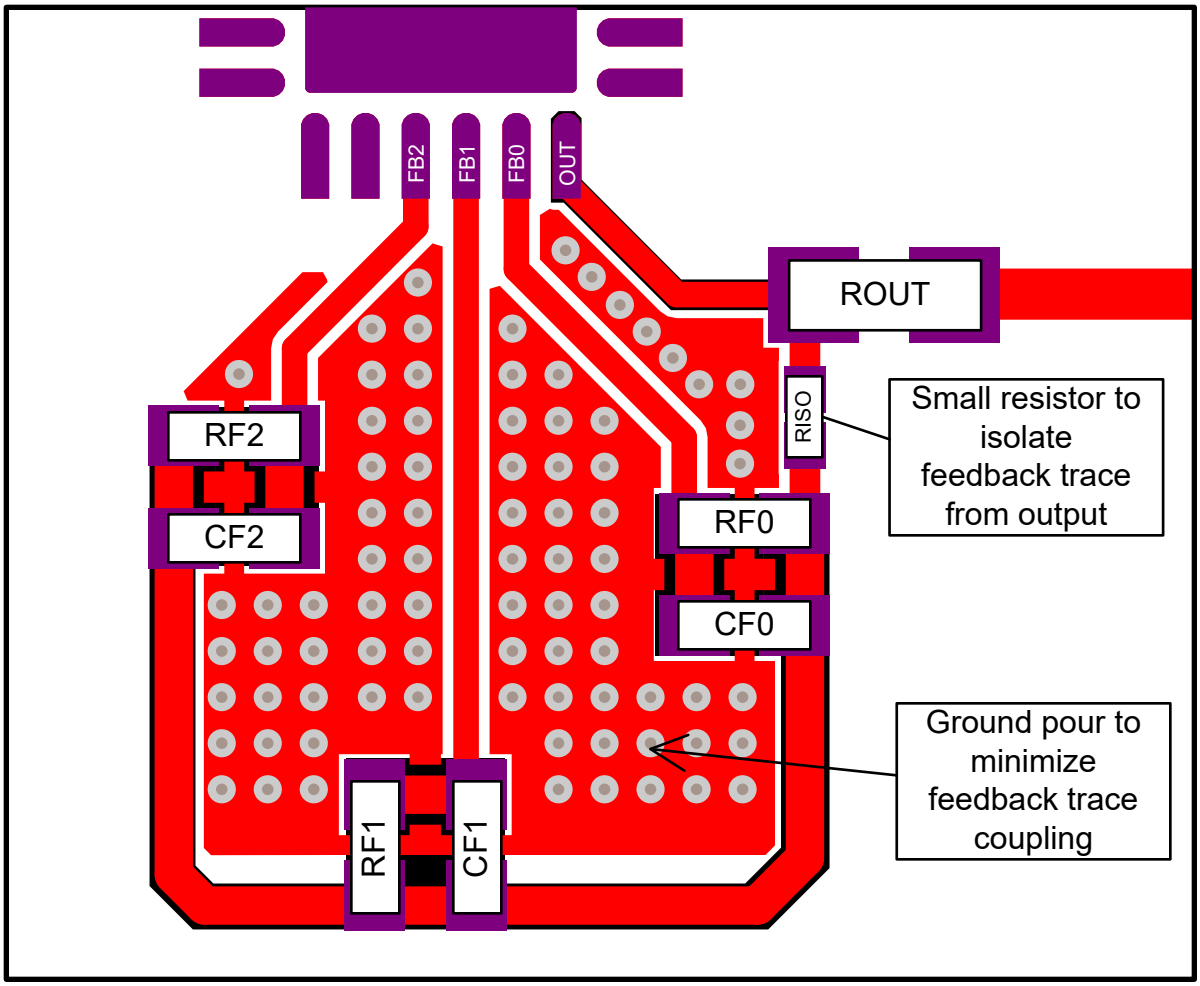

図 11-2. Feedback Network Layout Recommendations

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

- Texas Instruments, *Optical Front-End System Reference Design* design guide
- Texas Instruments, *LIDAR-Pulsed Time-of-Flight Reference Design Using High-Speed Data Converters* design guide
- Texas Instruments, *LIDAR Pulsed Time of Flight Reference Design* design guide

12.2 Documentation Support

12.2.1 Related Documentation

See the following for related documentation:

- Texas Instruments, *OPA3S2859-EP Evaluation Module* user's guide
- Texas Instruments, *Transimpedance Considerations for High-Speed Amplifiers* application report
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 1* blog
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 2* blog
- Texas Instruments, *Training Video: How to Design Transimpedance Amplifier Circuits*
- Texas Instruments, *Training Video: High-Speed Transimpedance Amplifier Design Flow*
- Texas Instruments, *Training Video: How to Convert a TINA-TI Model into a Generic SPICE Model*

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 サポート・リソース

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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA3S2859MRTWREP	ACTIVE	WQFN	RTW	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	3S2859	Samples
V62/22603-01XE	ACTIVE	WQFN	RTW	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		3S2859	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF OPA3S2859-EP :

- Catalog : OPA3S2859

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

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