INA741 85V、20 ビット、超高精度 I²C 出力デジタル電力モニタ、EZShunt™ テクノロジー搭載

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1 特長

- 低損失の内蔵シャント抵抗
  - 内部抵抗:800µΩ、T_A = 25℃
  - 連続電流:±35A、T_A = 25℃
  - ピーク測定機能:±39.32A
- 広い同相電圧範囲:-0.1V～+85V
- 高分解能、20 ビット・デルタ・シグマ ADC
- 電流監視精度:
  - オフセット電流:±5.5mA、最大値
  - オフセットのドリフト:±15µA/℃、最大値
  - システム・ゲイン誤差:25A で ±0.4%
  - システム・ゲイン誤差ドリフト:±25PPM/℃、代表値
  - 同相除去:±100µA/V、最大値
- 電力監視精度:
  - 25℃、フルスケールで±0.4%
- エネルギーと電荷量の精度:
  - 25℃、フルスケールで±0.9%
- 入力バイアス電流:2.5nA (最大値)
- 温度センサ:±1.5℃ (25℃時の最大値)
- 変換時間と平均化をプログラム可能
- 2.94MHz 高速 I²C インターフェイス、16 ピンで選択可能なアドレス付き
- 2.7V～5.5V 電源で動作:
  - 動作時電流:640µA (代表値)
  - シャットダウン電流:5µA (最大値)

2 アプリケーション

- 電力供給
- グリッド・インフラストラクチャ
- 産業用バッテリ・パック
- 試験用機器
- 通信機器
- エンタープライズ・サーバー

3 概要

INA741 は、電流検出素子を内蔵したデジタル電力モニタであり、電流センシング・アプリケーション向けに特別に設計された 20 ビット・デルタ・シグマ ADC も搭載しています。このデバイスは、-0.1V～+85V の同相電圧をサポートし、最大±39.32A のフルスケール電流を測定できます。

INA741 は、±0.5% の高精度内蔵発振器を使用しながら、電流、バス電圧、ダイ温度、電力、エネルギー、電荷の蓄積量を報告すると同時に、必要な計算をバックグラウンドで実行します。内蔵の温度センサは、接合部温度範囲全体にわたって ±2.5℃ の精度を維持します。

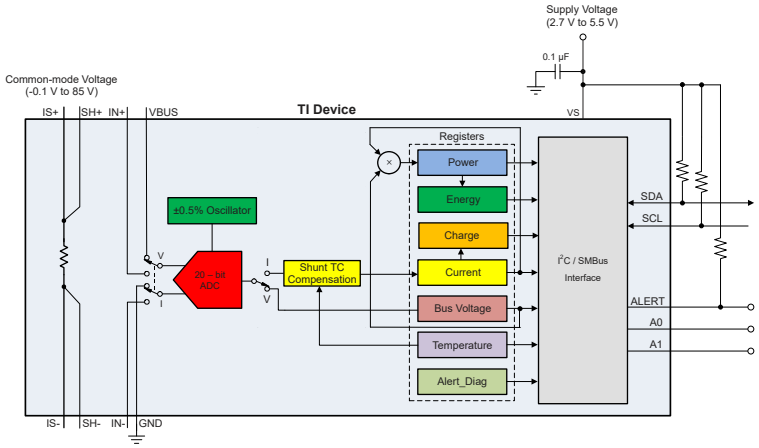
INA741 は低オフセットおよび低ゲイン・ドリフト設計のため、このデバイスは製造時に複数の温度較正を行わない正確なシステムで使用できます。

このデバイスでは、50µs から 4.12ms までの ADC 変換時間を選択でき、1x から 1024x までのサンプル平均化を行うことで、測定データのノイズをさらに減らすことができます。

パッケージ情報

部品番号	パッケージ(1)	パッケージサイズ (公称)(2)
INA741	REM (QFN、14)	5.00mm × 4.00mm

(1) 利用可能なパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。
(2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



概略ブロック図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
July 2023	*	Initial Release

5 Pin Configuration and Functions

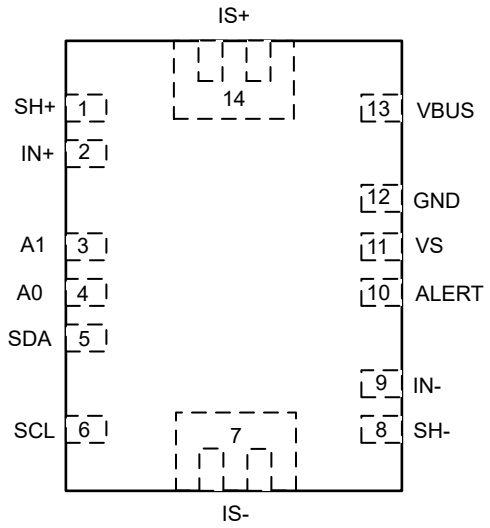

図 5-1. REM Package 14-Pin QFN Top View

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	SH+	Analog output	Shunt positive sense connection
2	IN+	Analog input	Positive input to digital power monitor.
3	A1	Digital input	I^2C address pin. Connect to GND, SCL, SDA, or VS.
4	A0	Digital input	I^2C address pin. Connect to GND, SCL, SDA, or VS.
5	SDA	Digital input/output	Open-drain bidirectional I^2C data.
6	SCL	Digital input	I^2C clock input.
7	IS–	Analog input	Negative high current shunt connection.
8	SH–	Analog output	Shunt negative sense connection.
9	IN–	Analog input	Negative input to digital power monitor.
10	ALERT	Digital output	Open-drain alert output, default state is active low.
11	VS	Power supply	Power supply, 2.7 V to 5.5 V.
12	GND	Ground	Ground.
13	VBUS	Analog input	Bus voltage input.
14	IS+	Analog input	Positive high current shunt connection.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage		6	V
V_{IN+}, V_{IN-} (2)	Common mode voltage	–0.3	85	V
V_{ALERT}	ALERT	–0.3	Vs + 0.3	V
V_{IO}	SDA, SCL	–0.3	6	V
I_{IN}	Input current into any pin, excluding IS+ and IS–		5	mA
I_{OUT}	Digital output current		10	mA
T_J	Junction temperature		165	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) VIN+ and VIN– are the voltages at the IN+ and IN– pins, respectively.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage	–0.1		85	V
V_S	Operating supply voltage	2.7		5.5	V
T_A	Specified ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1) (2)		INA741 REM (QFN) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	82.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	6.2	°C/W
Y_{JB}	Junction-to-board characterization parameter	81.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

(2) Thermal metrics are relative to the internal die and are conservative relative to the heating that would occur from the package leadframe shunt. For more details on heating, see the Safe Operating Area section.

6.5 Electrical Characteristics

at T_A = 25 °C, V_S = 3.3 V, I_{SENSE} = 0 A, V_{CM} = $V_{IN–}$ = V_{BUS}= 48 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
CMRR	Common-mode rejection	–0.1 V < V_{CM} < 85 V, T_A = –40°C to +125°C		±8	±100	µA/V
I_{os}	Input offset current	T_{CT} > 280 µs		±0.5	±5.5	mA
dV_{os}/dT	Input offset current drift	T_A = –40°C to +125°C		±2.5	±15	µA/°C
PSRR	Input offset current vs power supply	V_S = 2.7 V to 5.5 V, T_A = –40°C to +125°C		±0.1	±6	mA/V
V_{os_bus}	V_{BUS} offset voltage	V_{BUS} = 20 mV		±1	±3.5	mV
dV_{os}/dT	V_{BUS} offset voltage drift	T_A = –40°C to +125°C		±4	±20	µV/°C
PSRR	V_{BUS} offset voltage vs power supply	V_S = 2.7 V to 5.5 V		±1.1	3	mV/V
DC ACCURACY						
G_{SERR}	System current sense gain error	I_{SENSE} = –±25 A, V_{CM} = 24 V, T_A = 25°C		±0.01	±0.4	%
G_{S_DRFT}	System current sense gain error drift	–40°C ≤ T_A ≤ 125°C		±25		ppm/°C
G_{BERR}	V_{BUS} voltage gain error	V_{BUS} = 0 V to 85 V		±0.01	±0.1	%
		V_{BUS} = 0 V to 85 V, –40°C ≤ T_A ≤ 125°C		±0.025	±0.3	%
G_{B_DRFT}	V_{BUS} voltage gain error drift	–40°C ≤ T_A ≤ 125°C			±20	ppm/°C
Z_{BUS}	VBUS pin input impedance	Device enabled with active conversions		1		MΩ
P_{TME}	Power total measurement error (TME)	T_A = 25°C, at full scale			±0.4	%
E_{TME}	Energy and charge TME	at full scale power			±0.9	%
	ADC resolution			20		Bits
	1 LSB step size	Current		75		µA
		Bus voltage		195.3125		µV
		Temperature		7.8125		m°C
		Power		240		µW
		Energy		3.84		mJ
		Charge		75		µC
T_{CT}	ADC conversion-time(1)	Conversion time field = 0h		50		µs
		Conversion time field = 1h		84		
		Conversion time field = 2h		150		
		Conversion time field = 3h		280		
		Conversion time field = 4h		540		
		Conversion time field = 5h		1052		
		Conversion time field = 6h		2074		
		Conversion time field = 7h		4120		
INL	Integral Non-Linearity	Internal ADC		±2		m%
DNL	Differential Non-Linearity	Internal ADC		0.2		LSB
CLOCK SOURCE						
F_{OSC}	Internal oscillator frequency			1		MHz
OSC_{TOL}	Internal oscillator frequency tolerance	T_A = 25°C			±0.5	%
		T_A = –40°C to +125°C			±1	%
TEMPERATURE SENSOR						
	Measurement range		–40		+165	°C

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at T_A = 25 °C, V_S = 3.3 V, I_{SENSE} = 0 A, V_{CM} = $V_{IN–}$ = V_{BUS}= 48 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Temperature accuracy	T_A = 25°C		±0.15	±1.5	°C
		T_A= –40°C to +125°C		±0.2	±2.5	°C
INTEGRATED SHUNT						
	Internal kelvin resistance	SH+ to SH–, T_A = 25°C	700	800	950	µΩ
	Pin to pin package resistance	IS+ to IS–, T_A = 25°C	800	1000	1300	µΩ
	Maximum continuous current	–40°C ≤ T_A ≤ 125°C			±25	A
	Short time overload change	I_{SENSE} = 50 A for 5 seconds		±0.05		%
	Change due to temperature cycling	–65°C ≤ T_A ≤ 150°C, 500 cycles		±0.1		%
	Resistance change to solder heat	260°C solder, 10 s		±0.1		%
	High temperature exposure change	1000 hours, T_A = 165°C		±0.15		%
	Cold temperature storage change	24 hours, T_A = –65°C		±0.025		%
POWER SUPPLY						
V_S	Supply voltage		2.7		5.5	V
V_{POR}	POR Voltage Level	Supply rising		1.28		V
I_Q	Quiescent current	V_{SENSE} = 0 V		640	750	µA
		V_{SENSE} = 0 V, T_A = –40°C to +125°C			1	mA
I_{QSD}	Quiescent current, shutdown	Shutdown mode		2.8	5	µA
T_{POR}	Device start-up time	Power-up (NPOR)		300		µs
		From shutdown mode		60		
DIGITAL INPUT / OUTPUT						
V_{IH}	Logic input level, high	SDA, SCL	1.2		5.5	V
V_{IL}	Logic input level, low		GND		0.4	V
V_{OL}	Logic output level, low	I_{OL} = 3 mA	GND		0.4	V
I_{IO_LEAK}	Digital leakage input current	0 ≤ V_{IN} ≤ V_S	–1		1	µA

(1) Subject to oscillator accuracy and drift

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6.6 Timing Requirements (I^2C)

		MIN	NOM	MAX	UNIT
I^2C BUS (FAST MODE)					
$F_{(SCL)}$	I^2C clock frequency	1		400	kHz
$t_{(BUF)}$	Bus free time between STOP and START conditions	600			ns
$t_{(HDSTA)}$	Hold time after a repeated START condition. After this period, the first clock is generated.	100			ns
$t_{(SUSTA)}$	Repeated START condition setup time	100			ns
$t_{(SUSTO)}$	STOP condition setup time	100			ns
$t_{(HDDAT)}$	Data hold time	10		900	ns
$t_{(SUDAT)}$	Data setup time	100			ns
$t_{(LOW)}$	SCL clock low period	1300			ns
$t_{(HIGH)}$	SCL clock high period	600			ns
t_F	Data fall time			300	ns
t_F	Clock fall time			300	ns
t_R	Clock rise time			300	ns
I^2C BUS (HIGH-SPEED MODE)					
$F_{(SCL)}$	I^2C clock frequency	10		2940	kHz
$t_{(BUF)}$	Bus free time between STOP and START conditions	160			ns
$t_{(HDSTA)}$	Hold time after a repeated START condition. After this period, the first clock is generated.	100			ns
$t_{(SUSTA)}$	Repeated START condition setup time	100			ns
$t_{(SUSTO)}$	STOP condition setup time	100			ns
$t_{(HDDAT)}$	Data hold time	10		125	ns
$t_{(SUDAT)}$	Data setup time	20			ns
$t_{(LOW)}$	SCL clock low period	200			ns
$t_{(HIGH)}$	SCL clock high period	60			ns
t_F	Data fall time			80	ns
t_F	Clock fall time			40	ns
t_R	Clock rise time			40	ns

6.7 Timing Diagram

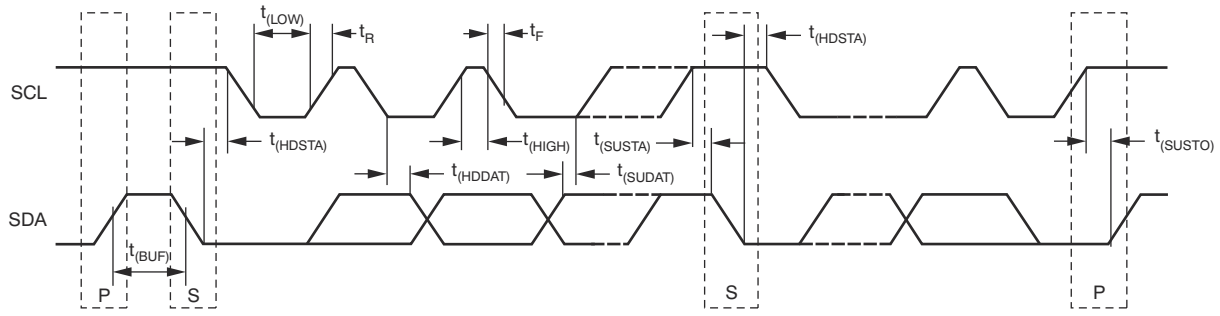


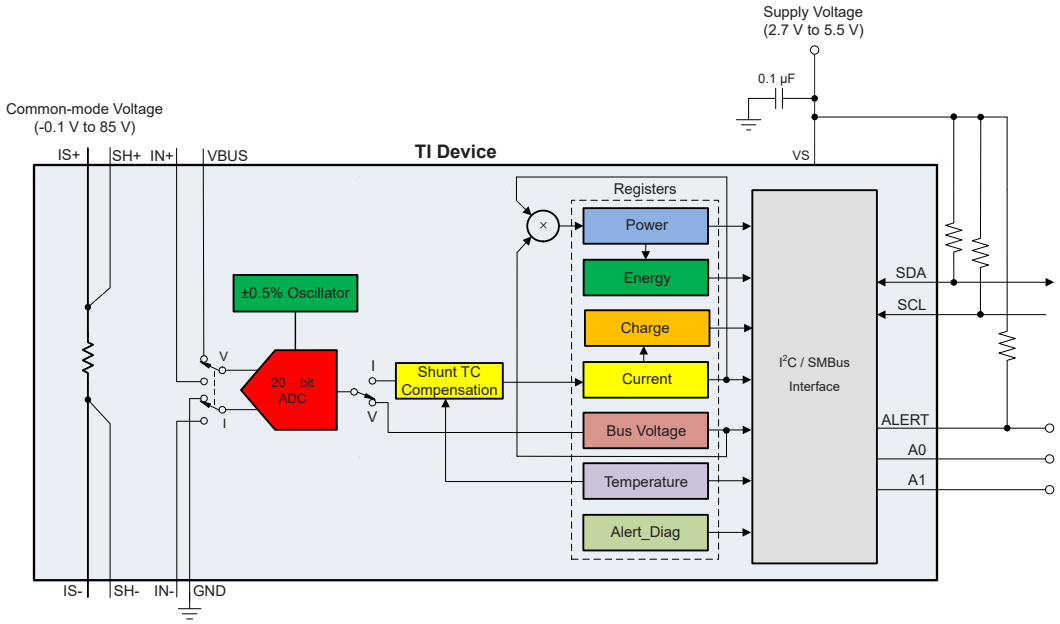
図 6-1. I^2C Timing Diagram

7 Detailed Description

7.1 Overview

The INA741 device is a digital current sense amplifier with an integrated current sensing element. The device measures current, bus voltage and internal temperature while calculating power, energy and charge necessary for accurate decision making in precisely controlled systems. Programmable registers allow flexible configuration for measurement precision as well as continuous or triggered operation. Detailed register information is found in *Register Maps*.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Integrated Shunt Resistor

The INA741 is a precise, low-drift, digital power monitor that provides accurate measurements over the entire specified ambient temperature range of –40°C to +125°C. The integrated current-sensing resistor is internally compensated to provide measurement stability over temperature, while simplifying printed circuit board (PCB) layout and size constraints.

Access to the on-chip current-sensing resistor is provided by the IS+ and IS- pins. This resistor features internal sense connections that are brought out on the SH+ and SH- pins. Access to the digital power monitor is provided by the IN+ and IN- pins. When the shunt sense connections are connected to the digital power monitor inputs, the sensed voltage is calibrated and temperature compensated to achieve a high level of accuracy. The construction of this resistor does not allow it to be used as a stand-alone component for accurate current measurement. The INA741 is system-calibrated to ensure that the current-sensing resistor and digital power monitor are both precisely matched to one another.

The nominal pin-to-pin resistance from IS+ to IS- is approximately 900 µΩ, while the internal resistance seen by the SH+ and SH- pins is nominally 800 µΩ. The power dissipation requirements of the system and package are based on the total package resistance between the IS+ and IS– pins.

7.3.2 Safe Operating Area

The heat generated by the device power dissipation limits the maximum current that can be safely handled by the package. The current consumed to power the device is low, therefore the primary source of heating is due to the current flow through the internal shunt resistor. The maximum safe-operating current level shown in 図 7-1 is

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set to ensure that the heat generated in the package is limited so that the internal junction temperature of the silicon does not exceed 165°C. This data was collected on the INA741 evaluation module (SENS108E1).

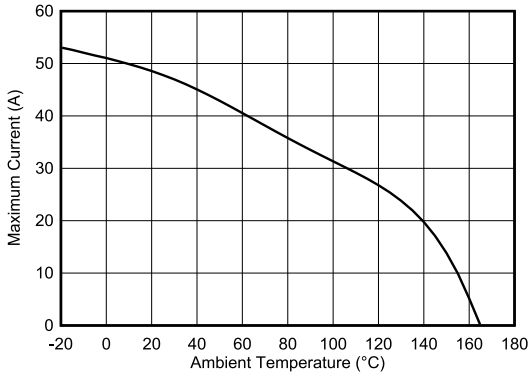

図 7-1. Maximum Continuous Shunt Current vs Ambient Temperature

Even though the shunt can withstand currents greater than 35 A, the current measurement capability is limited by ADC full scale range of 39.32 A. The ADC full scale range is also a function of temperature (see 図 8-1).

In applications with overcurrent transients, the peak amplitude and duration of the overcurrent event is important to determine the device heating. 図 7-2 shows the peak pulse current versus pulse duration that the device can withstand before the maximum junction temperature of 165°C is exceeded. The data shown in this curve was collected at T_A = 25°C, using the INA741 evaluation module (SENS108E1).

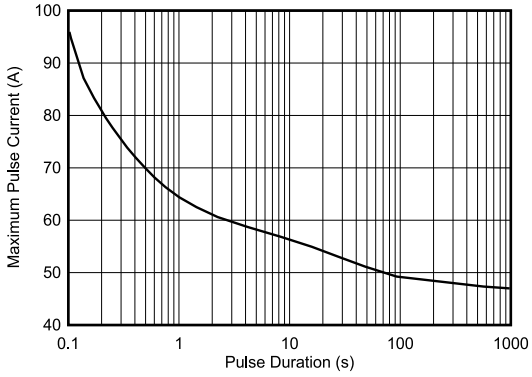

図 7-2. Maximum Pulse Current vs Pulse Duration (Single Event)

7.3.3 Versatile High Voltage Measurement Capability

The INA741 operates off a 2.7 V to 5.5 V supply but can measure voltage and current on rails as high as 85 V. The current is measured by sensing the voltage drop across an internal shunt resistor. The input stage of the INA741 is designed such that the input common-mode voltage can be higher than the device supply voltage, V_S. The common-mode voltage range at the inputs is -0.1 V to +85 V to support both high-side and low-side current measurements. There are no special considerations for power-supply sequencing because the common-mode input range and device supply voltage are independent of each other; therefore the bus voltage can be present with the supply voltage off (and vice-versa) without damaging the device.

The device also measures the bus supply voltage through the VBUS pin and temperature through the integrated temperature sensor. The voltage drop across the internal shunt resistor is measured by the IN+ and IN– pins, while the bus voltage is measured with respect to device ground. Monitored bus voltages can range from 0 V to 85 V, while monitored temperatures can range from –40°C to +165°C.

Shunt voltage, bus voltage, and internal temperature measurements are multiplexed internally to a single ADC (see 図 7-3).

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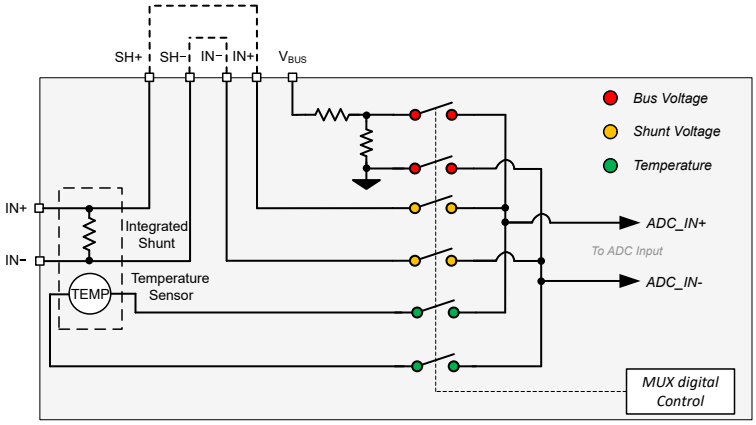

図 7-3. High-Voltage Input Multiplexer

7.3.4 Internal Measurement and Calculation Engine

The current and charge are calculated from the voltage drop measured across the internal resistive element, while the power and energy are calculated after a bus voltage measurement. Power and energy are calculated based on the previous current calculation and the latest bus voltage measurement.

The current, voltage, and temperature values are immediate results when the number of averages is set to 1 (see 図 7-4). However, when averaging is used, each ADC measurement is an intermediate result which is stored in the corresponding averaging registers. Following every ADC sample, the newly-calculated values for current, voltage, and temperature are appended to their corresponding averaging registers until the set number of averages is achieved. After all of the samples have been measured, the average current and voltage is determined, the power is calculated, and the results are loaded to the corresponding output registers where they can then be read.

The energy and charge values are accumulated for each conversion cycle. Therefore the INA741 averaging function is not applied to these.

Calculations for power, charge and energy are performed in the background and do not add to the overall conversion time.

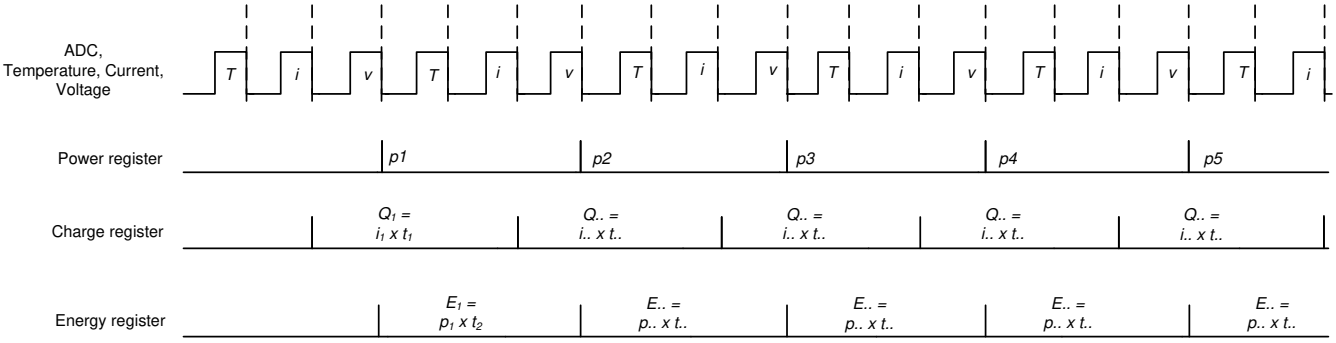

図 7-4. Power, Energy and Charge Calculation Scheme

7.3.5 High-Precision Delta-Sigma ADC

The integrated ADC is a high-performance, low-offset, low-drift, delta-sigma ADC designed to support bidirectional current measurement. The measured inputs are selected through the high-voltage input multiplexer to the ADC inputs (see 図 7-3). The ADC architecture enables lower drift measurement across temperature and consistent offset measurements across common-mode voltage, temperature, and power supply variations. A low-offset ADC is preferred in current sensing applications to provide a near 0 V offset voltage that maximizes the useful dynamic range of the system.

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The INA741 measures the die temperature, current, and bus voltage. An internal temperature measurement is made before each current measurement. Temperature compensation is then applied to the current measurement to achieve low drift performance. The MODE bits setting in the ADC_CONFIG register permit selecting modes to convert only the current or bus voltage to further allow the user to configure the monitoring function to fit the specific application requirements. After an ADC conversion is complete, the converted values independently update in their corresponding registers where they can be read through the digital interface at the time of conversion end if no averaging is selected. The conversion time for shunt voltage, bus voltage, and temperature inputs are set independently from 50 µs to 4.12 ms depending on the values programmed in the ADC_CONFIG register. The value for current is calculated after both the temperature and shunt voltage measurements are made. The total time to get the current measurement is the sum of the conversion times for these two parameters. Enabled measurement inputs are converted sequentially, which means the total time to convert all inputs depends on the conversion time for each input and the number of inputs enabled. When averaging is used, the intermediate values are subsequently stored in an averaging accumulator, and the conversion sequence repeats until the number of averages is reached. After all of the averaging is complete, the final values are updated in the corresponding registers that can then be read. These values remain in the data output registers until they are replaced by the next fully completed conversion results. In this case, reading the data output registers does not affect a conversion in progress.

The ADC has two conversion modes—continuous and triggered—set by the MODE bits in the ADC_CONFIG register. In continuous-conversion mode, the ADC will continuously convert the input measurements and update the output registers as described above in an indefinite loop. In triggered-conversion mode, the ADC will convert the input measurements as described above, after which the ADC will go into shutdown mode until another single-shot trigger is generated by writing to the MODE bits. Writing the MODE bits will interrupt and restart triggered or continuous conversions that are in progress. The values from the device can be read at any time because data from the last conversion remains available until the next conversion is complete. The Conversion Ready flag is set after all conversions and averaging are complete.

The Conversion Ready flag (CNVRF) clears under these conditions:

- Writing to the ADC_CONFIG register (except for selecting shutdown mode); or
- Reading the DIAG_ALRT Register

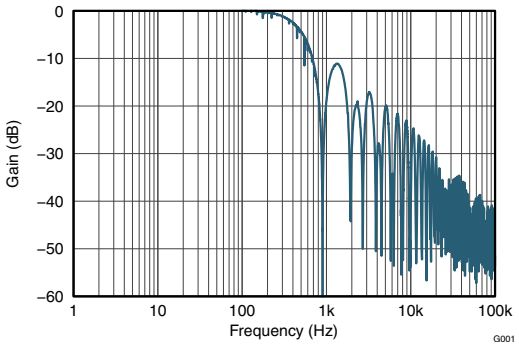
While the INA741 device is used in either one of the conversion modes, a dedicated digital engine is calculating the current, power, charge and energy values in the background as described in *Internal Measurement and Calculation Engine*. In triggered mode, the accumulation registers (ENERGY and CHARGE) are invalid, as the device does not keep track of elapsed time. For applications that require critical measurements in regards to accumulation of time for energy and charge measurements, the device must be configured to use continuous conversion mode, as the accumulated results are continuously updated and can provide true system representation of charge and energy consumption in a system. All of the calculations are performed in the background and do not contribute to conversion time.

For applications that must synchronize with other components in the system, the INA741 conversion can be delayed by programming the CONVDLY bits in the CONFIG register in the range between 0 ms (no delay) and 510 ms. The resolution in programming the conversion delay is 2 ms. The conversion delay is set to 0 ms by default. Conversion delay can assist in measurement synchronization when multiple external devices are used for voltage or current monitoring purposes. In applications where time-aligned voltage and current measurements are needed, two devices can be used with the current measurement delayed such that the external voltage and current measurements will occur at approximately the same time. Keep in mind that even though the internal time base for the ADC is precise, synchronization will be lost over time due to internal and external time base mismatch.

7.3.5.1 Low Latency Digital Filter

The device integrates a low-pass digital filter that performs both decimation and filtering on the ADC output data, which helps with noise reduction. The digital filter is automatically adjusted for the different output data rates and always settles within one conversion cycle. The user has the flexibility to choose different output conversion time periods T_{CT} from 50 µs to 4.12 ms. With this configuration the first amplitude notch appears at the Nyquist frequency of the output signal which is determined by the selected conversion time period and defined as

f_{NOTCH}= 1 / (2 x T_{CT}). This means that the filter cut-off frequency will scale proportionally with the data output rate as described. 図 7-5 shows the filter response when the 1.052 ms conversion time period is selected.



Conversion time = 1.052 ms, single conversion only

図 7-5. ADC Frequency Response

7.3.5.2 Flexible Conversion Times and Averaging

ADC conversion times for bus voltage can be set independently from 50 µs to 4.12 ms. The total conversion time for current includes an additional conversion time for temperature, and can be varied from 100 µs to 8.24 ms. The flexibility in conversion time allows for robust operation in a variety of noisy environments. The device also allows for programmable averaging times from a single conversion all the way to an average of 1024 conversions. The amount of averaging selected applies uniformly to all active measurement inputs. The ADC_CONFIG register shown in 表 7-6 provides additional details on the supported conversion times and averaging modes. The INA741 effective resolution of the ADC can be increased by increasing the conversion time and increasing the number of averages. 図 7-6 and 図 7-7 shown below illustrate the effect of conversion time and averaging on a constant input signal.

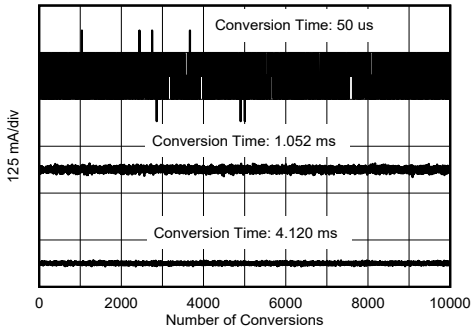


図 7-6. Noise vs Conversion Time (Averaging = 1)

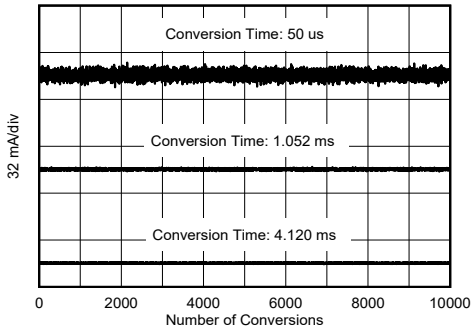


図 7-7. Noise vs Conversion Time (Averaging = 128)

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Settings for the conversion time and number of conversions averaged impact the effective measurement resolution. For more detailed information on how averaging reduces noise and increases the effective number of bits (ENOB) see *ADC Output Data Rate and Noise Performance*.

7.3.6 Integrated Precision Oscillator

The internal timebase of the device is provided by an internal oscillator that is trimmed to less than 0.5% tolerance at room temperature. The precision oscillator is the timing source for ADC conversions, as well as the time-count used for calculation of energy and charge. The digital filter response varies with conversion time; therefore the precise clock ensures filter response and notch frequency consistency across temperature. On power up, the internal oscillator and ADC take roughly 300 µs to reach <1% error stability. After the clock stabilizes, the ADC data output will be accurate to the electrical specifications provided in *Specifications*.

7.3.7 Multi-Alert Monitoring and Fault Detection

The INA741 includes a multipurpose, open-drain ALERT output pin that can be used to report multiple diagnostics, or to indicate that the ADC conversion is complete. The diagnostics listed in 表 7-1 are constantly monitored and can be reported through the ALERT pin whenever the monitored output value crosses the associated out-of-range threshold.

表 7-1. ALERT Diagnostics Description

INA741 DIAGNOSTIC	STATUS BIT IN DIAG_ALRT REGISTER (RO)	OUT-OF-RANGE THRESHOLD REGISTER (R/W)	REGISTER DEFAULT VALUE
Current Under-Limit	CURRENTUL	CUL	0x8000 h (two's complement)
Current Over-Limit	CURRENTOL	COL	0x7FFF h (two's complement)
Bus Voltage Over-Limit	BUSOL	BOVL	0x7FFF h (two's complement, positive values only)
Bus Voltage Under-Limit	BUSUL	BUVL	0x0000 h (two's complement, positive values only)
Temperature Over-Limit	TMPOL	TEMP_LIMIT	0xFFFF h (two's complement, positive values only)
Power Over-Limit	POL	PWR_LIMIT	0x7FFF h (two's complement)

A read of the DIAG_ALRT register is used to determine which diagnostic has triggered the ALERT pin. This register, shown in 表 7-13, is also used to monitor other associated diagnostics as well as configure some ALERT pin functions.

- Alert latch enable — In case the ALERT pin is triggered, this function will hold the value of the pin even after all diagnostic conditions have cleared. A read of the DIAG_ALRT register will reset the status of the ALERT pin. This function is enabled by setting the ALATCH bit.
- Conversion ready enable — Enables the ALERT pin to assert when an ADC conversion has completed and output values are ready to be read through the digital interface. This function is enabled by setting the CNVR bit. The conversion completed events can also be read through the CNVRF bit regardless of the CNVR bit setting.
- Alert comparison on averaged output — Allows the out-of-range threshold value to be compared to the averaged data values produced by the ADC. This helps to additionally remove noise from the output data when compared to the out-of-range threshold to avoid false alerts due to noise. However, the diagnostic will be delayed due to the time needed for averaging. This function is enabled by setting the SLOWALERT bit.
- Alert polarity — Allows the device to invert the active state of the ALERT pin. Note that the ALERT pin is an open-drain output that must be pulled up by a resistor. The ALERT pin is active-low by default and can be configured for active high function using the APOL control bit.

Other diagnostic functions that are not reported by the ALERT pin but are available by reading the DIAG_ALRT register:

- Math overflow — Indicated by the MATHOF bit, reports when an arithmetic operation has caused an internal register overflow.
- Memory status — Indicated by the MEMSTAT bit, monitors the health of the device non-volatile trim memory. This bit will always read '1' when the device is operating properly.
- Energy overflow — Indicated by the ENERGYOF bit, reports when the ENERGY register has reached an overflow state due to data accumulation.
- Charge overflow — Indicated by the CHARGEOF bit, reports when the CHARGE register has reached an overflow state due to data accumulation.

When the ALERT pin is configured to report the ADC conversion complete event, the ALERT pin becomes a multipurpose reporting output. 図 7-8 shows an example where the device reports ADC conversion complete events while the INA741 device is subject to an overcurrent event, bus undervoltage event, overtemperature event and over power-limit event.

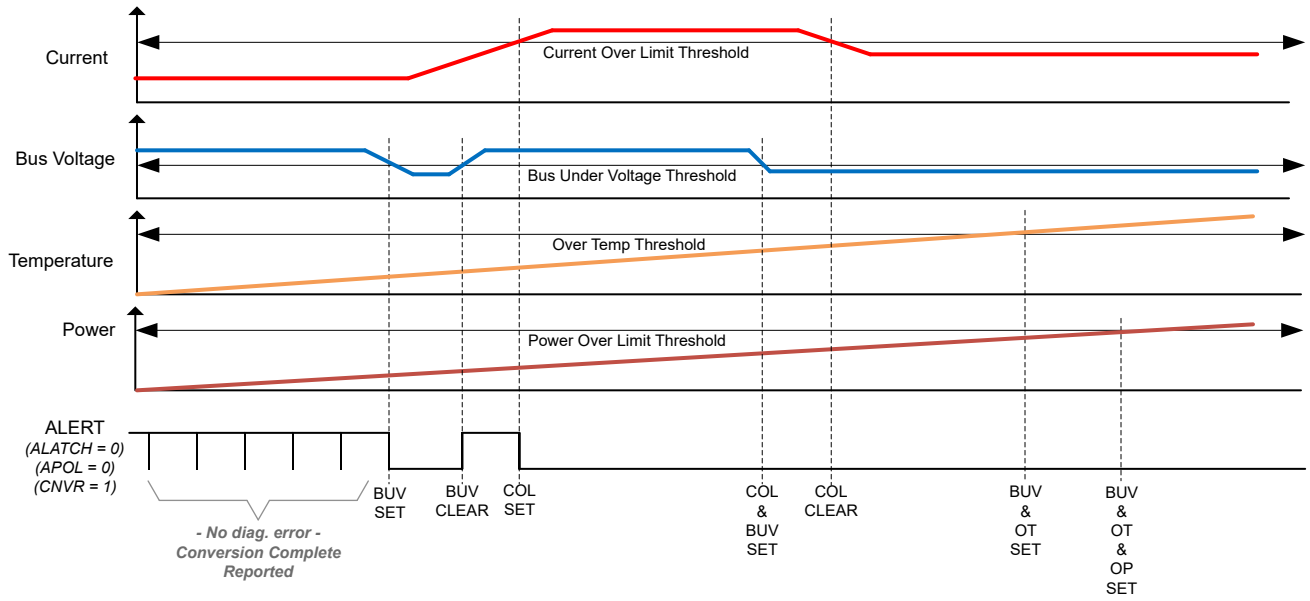

図 7-8. Multi-Alert Configuration

7.4 Device Functional Modes

7.4.1 Shutdown Mode

In addition to the two conversion modes (continuous and triggered), the device also has a shutdown mode (selected by the MODE bits in ADC_CONFIG register) that reduces the quiescent current to less than 5 µA and turns off current into the device inputs, reducing the impact of supply drain when the device is not being used. The registers of the device can be written to and read from while the device is in shutdown mode. The device remains in shutdown mode until another triggered conversion command or continuous conversion command is received.

The device can be triggered to perform conversions while in shutdown mode. When a conversion is triggered, the ADC will start the conversion. When the conversion completes, the device will return to the shutdown state.

Note that the shutdown current is specified with an inactive communications bus. Active clock and data activity will increase the current consumption as a function of the bus frequency.

7.4.2 Power-On Reset

Power-on reset (POR) is asserted when V_S drops below 1.26 V (typical) at which all of the registers are reset to their default values. A manual device reset can be initiated by setting the RST bit in the CONFIG register. The

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default power-up register values are shown in the reset column for each register description. Links to the register descriptions are shown in *Register Maps*.

7.5 Programming

7.5.1 I²C Serial Interface

The INA741 operates only as a target on both the SMBus and I²C interfaces. Connections to the bus are made through the open-drain SDA and SCL lines. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. Although the device integrates spike suppression into the digital I/O lines, proper layout techniques help minimize the amount of coupling into the communication lines. This noise introduction could occur from capacitive coupling signal edges between the two communication lines themselves or from other switching noise sources present in the system. Routing traces in parallel with ground in between layers on a printed circuit board (PCB) typically reduces the effects of coupling between the communication lines. Shielded communication lines reduce the possibility of unintended noise coupling into the digital I/O lines that could be incorrectly interpreted as start or stop commands.

The INA741 supports the transmission protocol for fast mode (1 kHz to 400 kHz) and high-speed mode (1 kHz to 2.94 MHz). All data bytes are transmitted most significant byte first and follow the SMBus 3.0 transfer protocol.

To communicate with the INA741, the controller must first address targets through a target address byte. The target address byte consists of seven address bits and a direction bit that indicates whether the action is to be a read or write operation.

The device has two address pins, A0 and A1. 表 7-2 lists the pin logic levels for each of the 16 possible addresses. The device samples the state of pins A0 and A1 on every bus communication. Establish the pin state before any activity on the interface occurs. When connecting the SDA pin to either A0 or A1 to set the device address, additional hold time of 100 ns is needed on the MSB of the I²C address to insure correct device addressing.

表 7-2. Address Pins and Target Addresses

A1	A0	TARGET DEVICE ADDRESS
GND	GND	1000000
GND	VS	1000001
GND	SDA	1000010
GND	SCL	1000011
VS	GND	1000100
VS	VS	1000101
VS	SDA	1000110
VS	SCL	1000111
SDA	GND	1001000
SDA	VS	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	VS	1001101
SCL	SDA	1001110
SCL	SCL	1001111

7.5.1.1 Writing to and Reading Through the I²C Serial Interface

Accessing a specific register on the INA741 is accomplished by writing the appropriate value to the register pointer. Refer to *Register Maps* for a complete list of registers and corresponding addresses. The value for the register pointer (as shown in 図 7-11) is the first byte transferred after the target address byte with the R/$\overline{W}$ bit low. Every write operation to the device requires a value for the register pointer.

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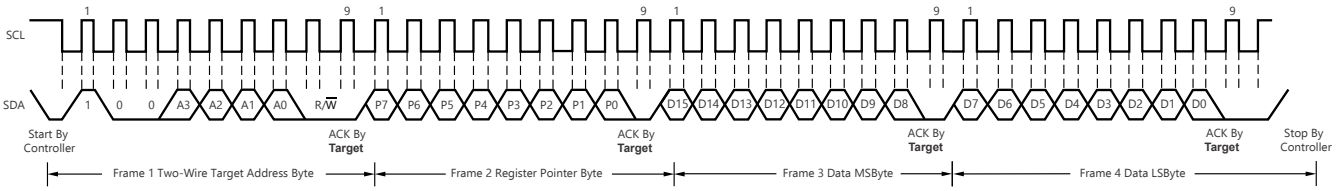
Writing to a register begins with the first byte transmitted by the controller. This byte is the target address, with the R/$\overline{W}$ bit low. The device then acknowledges receipt of a valid address. The next byte transmitted by the controller is the address of the register to be accessed. This register address value updates the register pointer to the desired internal device register. The next two bytes are written to the register addressed by the register pointer. The device acknowledges receipt of each data byte. The controller may terminate data transfer by generating a start or stop condition.

When reading from the device, the last value stored in the register pointer by a write operation determines which register is read during a read operation. To change the register pointer for a read operation, a new value must be written to the register pointer. This write is accomplished by issuing a target address byte with the R/$\overline{W}$ bit low, followed by the register pointer byte. No additional data are required. The controller then generates a start condition and sends the address byte for the target with the R/$\overline{W}$ bit high to initiate the read command. The next byte is transmitted by the target and is the most significant byte of the register indicated by the register pointer. This byte is followed by an *Acknowledge* from the controller; then the target transmits the least significant byte. The controller may or may not acknowledge receipt of the second data byte. The controller may terminate data transfer by generating a *Not-Acknowledge* after receiving any data byte, or generating a start or stop condition. If repeated reads from the same register are desired, it is not necessary to continually send the register pointer bytes; the device retains the register pointer value until it is changed by the next write operation.

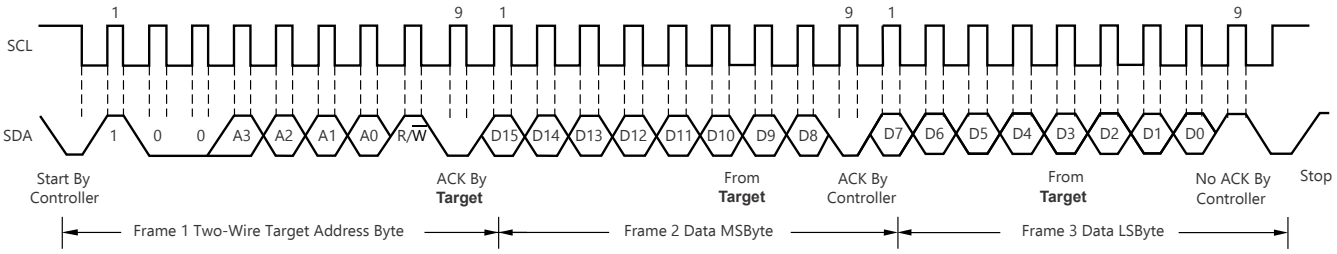
図 7-9 shows the write operation timing diagram. 図 7-10 shows the read operation timing diagram. These diagrams are shown for reading and writing to 16-bit registers. Registers with a higher number of bytes will behave similarly.

Register bytes are sent most significant byte (MSB) first, followed by the least significant byte (LSB).



A. The value of the target address byte is determined by the settings of the A0 and A1 pins. Refer to 表 7-2.
B. The device does not support packet error checking (PEC) or perform clock stretching.

図 7-9. Timing Diagram for Write Word Format



A. The value of the target address byte is determined by the settings of the A0 and A1 pins. Refer to 表 7-2.
B. Read data is from the last register pointer location. If a new register is desired, the register pointer must be updated. See 図 7-11.
C. ACK by the controller can also be sent.
D. The device does not support packet error checking (PEC) or perform clock stretching.

図 7-10. Timing Diagram for Read Word Format

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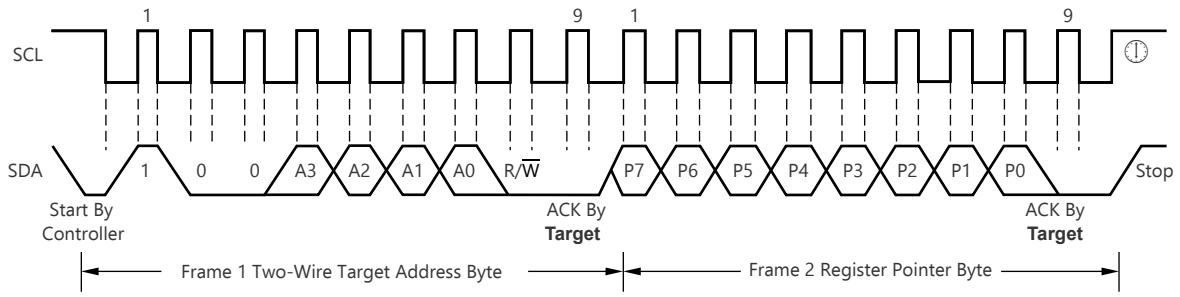

A. The value of the target address byte is determined by the settings of the A0 and A1 pins. Refer to 表 7-2.

図 7-11. Typical Register Pointer Set

7.5.1.2 High-Speed I²C Mode

When the bus is idle, both the SDA and SCL lines are pulled high by the pullup resistors. The controller generates a start condition followed by a valid serial byte containing high-speed (HS) controller code *00001XXX*. This transmission is made in fast (400 kHz) or standard (100 kHz) (F/S) mode at no more than 400 kHz. The INA741 does not acknowledge the HS controller code, but the INA741 does recognize the code and switches the internal filters to support 2.94-MHz operation.

The controller then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 2.94 MHz are allowed. Instead of using a stop condition, use repeated start conditions to maintain the bus in HS-mode. A stop condition ends the HS-mode and switches all the internal filters of the device to support the F/S mode.

7.5.1.3 SMBus Alert Response

The INA741 is designed to respond to the SMBus Alert Response address. The SMBus Alert Response provides a quick fault identification for simple targets. When an Alert occurs, the controller can broadcast the Alert Response target address (0001 100) with the Read/Write bit set high. Following this Alert Response, any target that generates an alert identifies itself by acknowledging the Alert Response and sending its address on the bus.

The Alert Response can activate several different targets simultaneously, similar to the I²C General Call. If more than one target attempts to respond, bus arbitration rules apply. The losing device does not generate an Acknowledge and continues to hold the Alert line low until that device wins arbitration.

7.6 Register Maps

7.6.1 INA741 Registers

表 7-3 lists the INA741 registers. All register locations not listed in 表 7-3 should be considered as reserved locations and the register contents should not be modified.

表 7-3. INA741 Registers

Address	Acronym	Register Name	Register Size (bits)	Section
0h	CONFIG	Configuration	16	Go
1h	ADC_CONFIG	ADC Configuration	16	Go
5h	VBUS	Bus Voltage Measurement	24	Go
6h	DIETEMP	Temperature Measurement	16	Go
7h	CURRENT	Current Result	24 (4 reserved)	Go
8h	POWER	Power Result	24	Go
9h	ENERGY	Energy Result	40	Go
Ah	CHARGE	Charge Result	40	Go
Bh	DIAG_ALRT	Diagnostic Flags and Alert	16	Go
Ch	COL	Current Over-Limit Threshold	16	Go

表 7-3. INA741 Registers (continued)

Address	Acronym	Register Name	Register Size (bits)	Section
Dh	CUL	Current Under-Limit Threshold	16	Go
Eh	BOVL	Bus Overvoltage Threshold	16	Go
Fh	BUVL	Bus Undervoltage Threshold	16	Go
10h	TEMP_LIMIT	Temperature Over-Limit Threshold	16	Go
11h	PWR_LIMIT	Power Over-Limit Threshold	16	Go
3Eh	MANUFACTURER_ID	Manufacturer ID	16	Go

Complex bit access types are encoded to fit into small table cells. 表 7-4 shows the codes that are used for access types in this section.

表 7-4. INA741 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.1.1 Configuration (CONFIG) Register (Address = 0h) [reset = 0h]

The CONFIG register is shown in 表 7-5.

Return to the Summary Table.

表 7-5. CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RST	R/W	0h	Reset Bit. Setting this bit to '1' generates a system reset that is the same as power-on reset. Resets all registers to default values. 0h = Normal Operation 1h = System Reset sets registers to default values This bit self-clears.
14	RSTACC	R/W	0h	Resets the contents of accumulation registers ENERGY and CHARGE to 0 0h = Normal Operation 1h = Clears registers to default values for ENERGY and CHARGE registers
13-6	CONVDLY	R/W	0h	Sets the Delay for initial ADC conversion in steps of 2 ms. 0h = 0 s 1h = 2 ms FFh = 510 ms
5	RESERVED	R	0h	Reserved. Always reads 0.
4	RESERVED	R	1h	Reserved. Always reads 1.
3-0	RESERVED	R	0h	Reserved. Always reads 0.

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7.6.1.2 ADC Configuration (ADC_CONFIG) Register (Address = 1h) [reset = FB68h]

The ADC_CONFIG register is shown in 表 7-6.

Return to the Summary Table.

表 7-6. ADC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	MODE	R/W	Fh	The user can set the MODE bits for continuous or triggered mode on bus voltage, shunt voltage or temperature measurement. 0h = Shutdown 1h = Triggered bus voltage, single shot 2h = Reserved 3h = Reserved 4h = Triggered temperature, single shot 5h = Triggered temperature and bus voltage, single shot 6h = Triggered temperature and current, single shot 7h = Triggered temperature, current and bus voltage, single shot 8h = Shutdown 9h = Continuous bus voltage only Ah = Reserved Bh = Reserved Ch = Continuous temperature only Dh = Continuous bus voltage and temperature Eh = Continuous temperature and current Fh = Continuous temperature, current, and bus voltage
11-9	VBUSCT	R/W	5h	Sets the conversion time of the bus voltage measurement. 0h = 50 µs 1h = 84 µs 2h = 150 µs 3h = 280 µs 4h = 540 µs 5h = 1052 µs 6h = 2074 µs 7h = 4120 µs
8-6	VSENCT	R/W	5h	Sets the conversion time of the shunt resistor voltage. Works in conjunction with the temperature conversion time. Total conversion time for a current measurement is the sum of VSENCT and TCT selections. 0h = 50 µs 1h = 84 µs 2h = 150 µs 3h = 280 µs 4h = 540 µs 5h = 1052 µs 6h = 2074 µs 7h = 4120 µs

表 7-6. ADC_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-3	TCT	R/W	5h	Sets the conversion time of the temperature measurement. Works in conjunction with the shunt voltage conversion time for current measurements. Total conversion time for a current measurement is the sum of VSENCT and TCT selections. 0h = 50 µs 1h = 84 µs 2h = 150 µs 3h = 280 µs 4h = 540 µs 5h = 1052 µs 6h = 2074 µs 7h = 4120 µs
2-0	AVG	R/W	0h	Selects ADC sample averaging count. The averaging setting applies to all active inputs. When >0h, the output registers are updated after the averaging has completed. 0h = 1 1h = 4 2h = 16 3h = 64 4h = 128 5h = 256 6h = 512 7h = 1024

7.6.1.3 Bus Voltage Measurement (VBUS) Register (Address = 5h) [reset = 0h]

The VBUS register is shown in 表 7-7.

Return to the Summary Table.

表 7-7. VBUS Register Field Descriptions

Bit	Field	Type	Reset	Description
23-4	VBUS	R	0h	Bus voltage output. Two's complement value, however always positive. Conversion factor: 195.3125 µV/LSB
3-0	RESERVED	R	0h	Reserved. Always reads 0.

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7.6.1.4 Temperature Measurement (DIETEMP) Register (Address = 6h) [reset = 0h]

The DIETEMP register is shown in 表 7-8.

Return to the Summary Table.

表 7-8. DIETEMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DIETEMP	R	0h	Internal die temperature measurement. Two's complement value. Conversion factor: 7.8125 m°C/LSB

7.6.1.5 Current Result (CURRENT) Register (Address = 7h) [reset = 0h]

The CURRENT register is shown in 表 7-9.

Return to the Summary Table.

表 7-9. CURRENT Register Field Descriptions

Bit	Field	Type	Reset	Description
23-4	CURRENT	R	0h	Calculated current output in Amperes. Two's complement value. Conversion factor: 75 µA/LSB.
3-0	RESERVED	R	0h	Reserved. Always reads 0.

7.6.1.6 Power Result (POWER) Register (Address = 8h) [reset = 0h]

The POWER register is shown in 表 7-10.

Return to the Summary Table.

表 7-10. POWER Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	POWER	R	0h	Calculated power output. Output value in Watts. Unsigned representation. Positive value. Conversion factor: 240 µW/LSB.

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7.6.1.7 Energy Result (ENERGY) Register (Address = 9h) [reset = 0h]

The ENERGY register is shown in 表 7-11.

Return to the Summary Table.

表 7-11. ENERGY Register Field Descriptions

Bit	Field	Type	Reset	Description
39-0	ENERGY	R	0h	Calculated energy output. Output value is in Joules.Unsigned representation. Positive value. Conversion factor: 3.84 mJ/LSB.

7.6.1.8 Charge Result (CHARGE) Register (Address = Ah) [reset = 0h]

The CHARGE register is shown in 表 7-12.

Return to the Summary Table.

表 7-12. CHARGE Register Field Descriptions

Bit	Field	Type	Reset	Description
39-0	CHARGE	R	0h	Calculated charge output. Output value is in Coulombs.Two's complement value. Conversion factor: 75 µC//LSB.

7.6.1.9 Diagnostic Flags and Alert (DIAG_ALRT) Register (Address = Bh) [reset = 0001h]

The DIAG_ALRT register is shown in 表 7-13.

Return to the Summary Table.

表 7-13. DIAG_ALRT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ALATCH	R/W	0h	When the Alert Latch Enable bit is set to Transparent mode, the Alert pin and Flag bit reset to the idle state when the fault has been cleared. When the Alert Latch Enable bit is set to Latch mode, the Alert pin and Alert Flag bit remain active following a fault until the DIAG_ALRT Register has been read. 0h = Transparent 1h = Latched
14	CNVR	R/W	0h	Setting this bit high configures the Alert pin to be asserted when the Conversion Ready Flag (bit 1) is asserted, indicating that a conversion cycle has completed. 0h = Disables conversion ready flag on ALERT pin 1h = Enables conversion ready flag on ALERT pin
13	SLOWALERT	R/W	0h	When enabled, ALERT function is asserted on the completed averaged value. This gives the flexibility to delay the ALERT until after the averaged value. 0h = ALERT comparison on non-averaged (ADC) value 1h = ALERT comparison on averaged value
12	APOL	R/W	0h	Alert Polarity bit sets the Alert pin polarity. 0h = Normal (active-low, open-drain) 1h = Inverted (active-high, open-drain)

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表 7-13. DIAG_ALRT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	ENERGYOF	R	0h	This bit indicates the health of the ENERGY register. If the 40-bit ENERGY register has overflowed this bit is set to 1. 0h = Normal 1h = Overflow Clears by setting the RSTACC field in the Configuration register.
10	CHARGEOF	R	0h	This bit indicates the health of the CHARGE register. If the 40-bit CHARGE register has overflowed this bit is set to 1. 0h = Normal 1h = Overflow Clears by setting the RSTACC field in the Configuration register.
9	MATHOF	R	0h	This bit is set to 1 if an arithmetic operation resulted in an overflow error. It indicates that current and power data may be invalid. 0h = Normal 1h = Overflow Must be manually cleared by triggering another conversion or by clearing the accumulators with the RSTACC bit.
8	RESERVED	R	0h	Reserved. Always read 0.
7	TMPOL	R/W	0h	This bit is set to 1 if the temperature measurement exceeds the threshold limit in the temperature over-limit register. 0h = Normal 1h = Overtemperature Event When ALATCH =1 this bit is cleared by reading this register.
6	CURRENTOL	R/W	0h	This bit is set to 1 if the current measurement exceeds the threshold limit in the current over-limit register. 0h = Normal 1h = Overcurrent Event When ALATCH =1 this bit is cleared by reading this register.
5	CURRENTUL	R/W	0h	This bit is set to 1 if the current measurement falls below the threshold limit in the current under-limit register. 0h = Normal 1h = Undercurrent Event When ALATCH =1 this bit is cleared by reading this register.
4	BUSOL	R/W	0h	This bit is set to 1 if the bus voltage measurement exceeds the threshold limit in the bus over-limit register. 0h = Normal 1h = Bus Over-Limit Event When ALATCH =1 this bit is cleared by reading this register.
3	BUSUL	R/W	0h	This bit is set to 1 if the bus voltage measurement falls below the threshold limit in the bus under-limit register. 0h = Normal 1h = Bus Under-Limit Event When ALATCH =1 this bit is cleared by reading this register.
2	POL	R/W	0h	This bit is set to 1 if the power measurement exceeds the threshold limit in the power limit register. 0h = Normal 1h = Power Over-Limit Event When ALATCH =1 this bit is cleared by reading this register.
1	CNVRF	R/W	0h	This bit is set to 1 if the conversion is completed. 0h = Normal 1h = Conversion is complete When ALATCH =1 this bit is cleared by reading this register or starting a new triggered conversion.

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表 7-13. DIAG_ALRT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MEMSTAT	R/W	1h	This bit is set to 0 if a checksum error is detected in the device trim memory space. 0h = Memory Checksum Error 1h = Normal Operation

7.6.1.10 Current Over-Limit Threshold (COL) Register (Address = Ch) [reset = 7FFFh]

If negative values are entered in this register, then a current measurement of 0 A will trip this alarm. When using negative values for the undercurrent and overcurrent thresholds be aware that the overcurrent threshold must be set to the larger (that is, less negative) of the two values. The COL register is shown in 表 7-14.

Return to the Summary Table.

表 7-14. COL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	COL	R/W	7FFFh	Sets the threshold for comparison of the value to detect over current condition (overcurrent protection). Two's complement value. Conversion factor: 1.2 mA/LSB

7.6.1.11 Current Under-Limit Threshold (CUL) Register (Address = Dh) [reset = 8000h]

The CUL register is shown in 表 7-15.

Return to the Summary Table.

表 7-15. CUL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CUL	R/W	8000h	Sets the threshold for comparison of the value to detect undercurrent condition. Two's complement value. Conversion factor: 1.2 mA/LSB

7.6.1.12 Bus Overvoltage Threshold (BOVL) Register (Address = Eh) [reset = 7FFFh]

The BOVL register is shown in 表 7-16.

Return to the Summary Table.

表 7-16. BOVL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	Reserved. Always reads 0.
14-0	BOVL	R/W	7FFFh	Sets the threshold for comparison of the value to detect Bus Overvoltage (overvoltage protection). Unsigned representation, positive value only. Conversion factor: 3.125 mV/LSB.

7.6.1.13 Bus Undervoltage Threshold (BUVL) Register (Address = Fh) [reset = 0h]

The BUVL register is shown in 表 7-17.

Return to the Summary Table.

表 7-17. BUVL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	Reserved. Always reads 0.
14-0	BUVL	R/W	0h	Sets the threshold for comparison of the value to detect Bus Undervoltage (undervoltage protection). Unsigned representation, positive value only. Conversion factor: 3.125 mV/LSB.

7.6.1.14 Temperature Over-Limit Threshold (TEMP_LIMIT) Register (Address = 10h) [reset = 7FFFh]

The TEMP_LIMIT register is shown in 表 7-18.

Return to the Summary Table.

表 7-18. TEMP_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TOL	R/W	7FFFh	Sets the threshold for comparison of the value to detect over temperature measurements. Two's complement value. The value entered in this field compares directly against the value from the DIETEMP register to determine if an overtemperature condition exists. Conversion factor: 7.8125 m°C/LSB.

7.6.1.15 Power Over-Limit Threshold (PWR_LIMIT) Register (Address = 11h) [reset = FFFFh]

The PWR_LIMIT register is shown in 表 7-19.

Return to the Summary Table.

表 7-19. PWR_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	POL	R/W	FFFFh	Sets the threshold for comparison of the value to detect power over-limit measurements. Unsigned representation, positive value only. The value entered in this field compares directly against the value from the POWER register to determine if an over-power condition exists. Conversion factor: 256 × Power LSB or 61.44 mW/LSB

7.6.1.16 Manufacturer ID (MANUFACTURER_ID) Register (Address = 3Eh) [reset = 5449h]

The MANUFACTURER_ID register is shown in 表 7-20.

Return to the Summary Table.

表 7-20. MANUFACTURER_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MANFID	R	5449h	Reads back TI in ASCII.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Device Measurement Range and Resolution

The INA741 has a full scale ADC range for current measurements of ±39.32 A. However, the maximum value that can be measured is limited by the operating junction temperature (see 図 8-1).

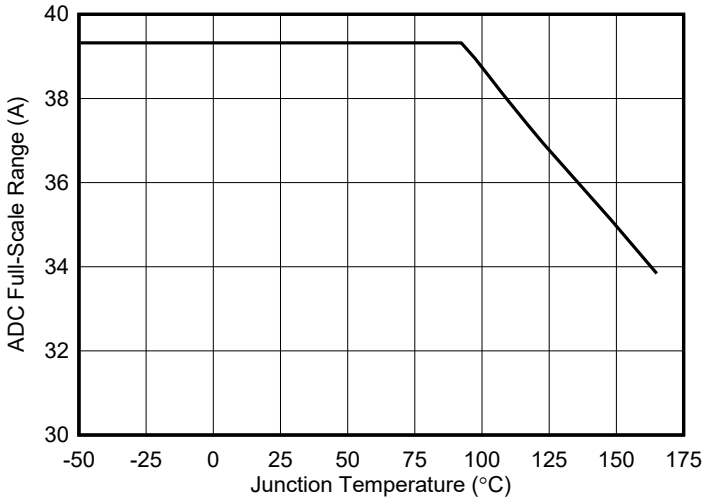

図 8-1. Maximum ADC Current Reading vs Junction Temperature

表 8-1 shows the full scale voltage on shunt, bus, and temperature measurements, along with their associated step size.

表 8-1. Register Full Scale Values and Resolution

PARAMETER	REGISTER ADDRESS	SIZE	FULL SCALE VALUE	RESOLUTION
Current	7h	20 bit, signed	±39.322	75 µA/LSB
Bus voltage	5h	20 bit, signed, always positive	0 V to 85 V	195.3125 µV/LSB
Die Temperature	6h	16 bit, signed	–40°C to +165°C	7.8125m°C/LSB
Power	8h	24 bit, unsigned	4026.53 kW	240 µW/LSB
Energy	9h	40 bit, unsigned	4222.12 MJ	3.84 mJ/LSB
Charge	Ah	40 bit, unsigned	82.46 MC	75 µC/LSB

The internal die temperature sensor register range extends from –256°C to +256°C but is limited by the junction temperature range of –40°C to 165°C. Likewise, the bus voltage measurement range extends up to 102.4 V but is limited by silicon to 85 V.

Current, bus voltage, temperature, power, energy and charge measurements can be read through their corresponding address registers. Values are calculated by multiplying the returned value by the corresponding LSB size.

Signed values are represented in two's compliment format.

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Upon overflow, the ENERGY register will roll over and start from zero. This register value can also be reset at any time by setting the RSTACC bit in the CONFIG register.

An overflow event in the CHARGE register is indicated by the CHARGEOF bit. If an overflow condition occurs, the CHARGE register needs to be manually reset by setting the RSTACC bit in the CONFIG register.

For a design example using these equations refer to *Detailed Design Procedure*.

8.1.2 ADC Output Data Rate and Noise Performance

The INA741 noise performance and effective resolution depend on the ADC conversion time. The device also supports digital averaging which can further help decrease digital noise. The flexibility of the device to select ADC conversion time and data averaging offers increased signal-to-noise ratio and achieves the highest dynamic range with lowest offset. The profile of the noise at lower signals levels is dominated by the system noise that is comprised mainly of 1/f noise or white noise. The INA741 effective resolution of the ADC can be increased by increasing the conversion time and increasing the number of averages.

表 8-2 summarizes the output data rate conversion settings supported by the device. The fastest conversion setting is 50 µs. Typical noise-free resolution is represented as Effective Number of Bits (ENOB) based on device measured data. The ENOB is calculated based on noise peak-to-peak values, which assures that full noise distribution is taken into consideration.

表 8-2. INA741 Noise Performance

ADC CONVERSION TIME PERIOD [µs]	OUTPUT SAMPLE AVERAGING [SAMPLES]	OUTPUT SAMPLE PERIOD [ms]	NOISE-FREE ENOB CURRENT MEASUREMENT
50	1	0.05	9.9
84		0.084	10.3
150		0.15	10.9
280		0.28	11.8
540		0.54	12.0
1052		1.052	12.5
2074		2.074	13.1
4120		4.12	13.7
50	4	0.2	11.1
84		0.336	11.3
150		0.6	12.1
280		1.12	12.7
540		2.16	13.2
1052		4.208	13.6
2074		8.296	14.0
4120		16.48	14.5
50	16	0.8	12.1
84		1.344	12.3
150		2.4	13.2
280		4.48	13.5
540		8.64	13.9
1052		16.832	14.6
2074		33.184	14.9
4120		65.92	15.4

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表 8-2. INA741 Noise Performance (continued)

ADC CONVERSION TIME PERIOD [µs]	OUTPUT SAMPLE AVERAGING [SAMPLES]	OUTPUT SAMPLE PERIOD [ms]	NOISE-FREE ENOB CURRENT MEASUREMENT
50	64	3.2	13.1
84		5.376	13.2
150		9.6	14.0
280		17.92	14.6
540		34.56	15.0
1052		67.328	15.4
2074		132.736	16.0
4120		263.68	16.4
50	128	6.4	13.7
84		10.752	13.7
150		19.2	14.3
280		35.84	15.3
540		69.12	15.5
1052		134.656	16.0
2074		265.472	16.5
4120		527.36	17.0
50	256	12.8	14.3
84		21.504	14.4
150		38.4	14.9
280		71.68	15.5
540		138.24	16.0
1052		269.312	16.6
2074		530.944	16.9
4120		1054.72	17.3
50	512	25.6	14.5
84		43	15.0
150		76.8	15.8
280		143.36	15.8
540		276.48	16.4
1052		538.624	17.1
2074		1061.888	17.7
4120		2109.44	17.7
50	1024	51.2	15.2
84		86.016	15.5
150		153.6	16.0
280		286.72	16.4
540		552.96	16.9
1052		1077.248	17.7
2074		2123.776	18.1
4120		4218.88	19.2

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8.2 Typical Application

The low offset voltage and low input bias current of the INA741 allow accurate monitoring of a wide range of currents. 図 8-2 shows a circuit example for monitoring currents in a high-side configuration.

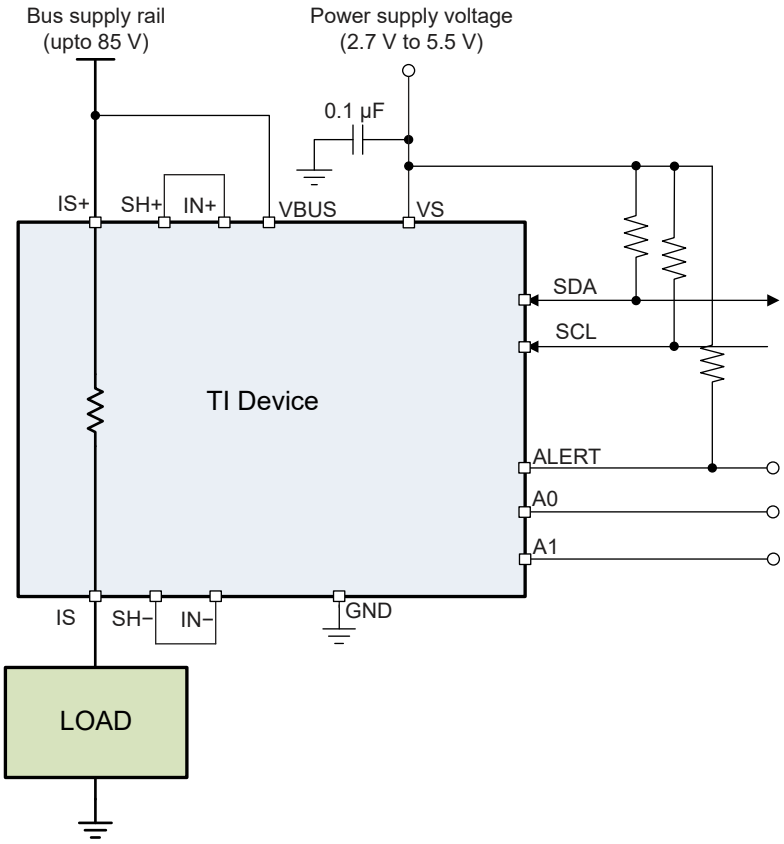

図 8-2. INA741 High-Side Sensing Application Diagram

8.2.1 Design Requirements

The design requirements for the circuit shown in 図 8-2 are listed in 表 8-3.

表 8-3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Power-supply voltage (V_S)	5 V
Bus supply rail (V_{CM})	48 V
Bus supply rail overvoltage fault threshold	54 V
Average Current	18 A
Overcurrent fault threshold (I_{MAX})	21 A
Temperature	85°C
Charge Accumulation Period	15 minutes

8.2.2 Detailed Design Procedure

8.2.2.1 Configure the Device

The first step to program the INA741 is to properly set the device and ADC configuration registers. On initial power up, the CONFIG and ADC_CONFIG registers are set to the reset values as shown in 表 7-5 and 表 7-6. In this default power-on state the device is set with the ADC continuously converting the temperature, current, and bus voltage. If the default power-up conditions do not meet the design requirements, these registers must be set properly after each V_S power cycle event.

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8.2.2.2 Set Desired Fault Thresholds

Fault thresholds are set by programming the desired trip threshold into the corresponding fault register. 表 7-1 lists the supported fault registers. The fault limit registers are 16 bits in length, therefore the effective LSB size for these registers is 16 times greater than the corresponding 20-bit LSB used in calculating returned values for bus voltage and current.

An overcurrent threshold is set by programming the Current Over-Limit Threshold register (COL). Divide the overcurrent limit value by the current LSB size to calculate the value needed to program the register.

In this example, the desired overcurrent limit threshold is 21 A. The Current LSB size is 75 µA/LSB, therefore the value that should be programmed into Current Over-Limit (COL) register is 40 A / (75 µA/LSB × 16) = 17500d or 445Ch.

An overvoltage fault threshold on the bus voltage is set by programming the bus overvoltage limit register (BOVL). In this example, the desired overvoltage threshold is 54 V. Divide the target threshold voltage by the correct LSB value to calculate the value needed to program the register. For this example, the target value for the BOVL register is = 17280d (4380h).

When setting the power over-limit value, the LSB size used to calculate the value needed in the limit registers will be 256 times greater than the power LSB. This is because the power register is 24 bits in length while the power fault limit register is 16 bits.

Values stored in the alert limit registers are set to the default values after V_S power cycle events and must be reprogrammed each time power is applied.

8.2.2.3 Calculate Returned Values

Multiply the returned value by the LSB value to calculate the parametric values. 表 8-4 below shows the returned values for this application example assuming the design requirements shown in 表 8-3.

表 8-4. Calculating Returned Values

PARAMETER	RETURNED VALUE	LSB VALUE	CALCULATED VALUE
Current (A)	240000d, 3 A980h	75 µA/LSB	18 A
Bus voltage (V)	245760d, 3 C000h	195.3125 µV/LSB	48 V
Power (W)	3600000d, 36 EE80h	240 µW/LSB	864 W
Energy (J)	202500000d, C11E7A0h	3.84 mJ/LSB	777600 J
Charge (C)	216000000d, CDF E600h	75 µC/LSB	16200 C
Temperature (°C)	10880d, 2A80h	7.8125 m°C/LSB	85°C

Current, Bus Voltage (positive only), Charge, and Temperature return values in two's complement format. In a two's complement format, a 1 in the most significant bit of the returned value represents a negative value in binary. These values can be converted to decimal by first inverting all the bits and adding 1 to obtain the unsigned binary value. This value must then be converted to decimal with the negative sign applied.

8.3 Power Supply Recommendations

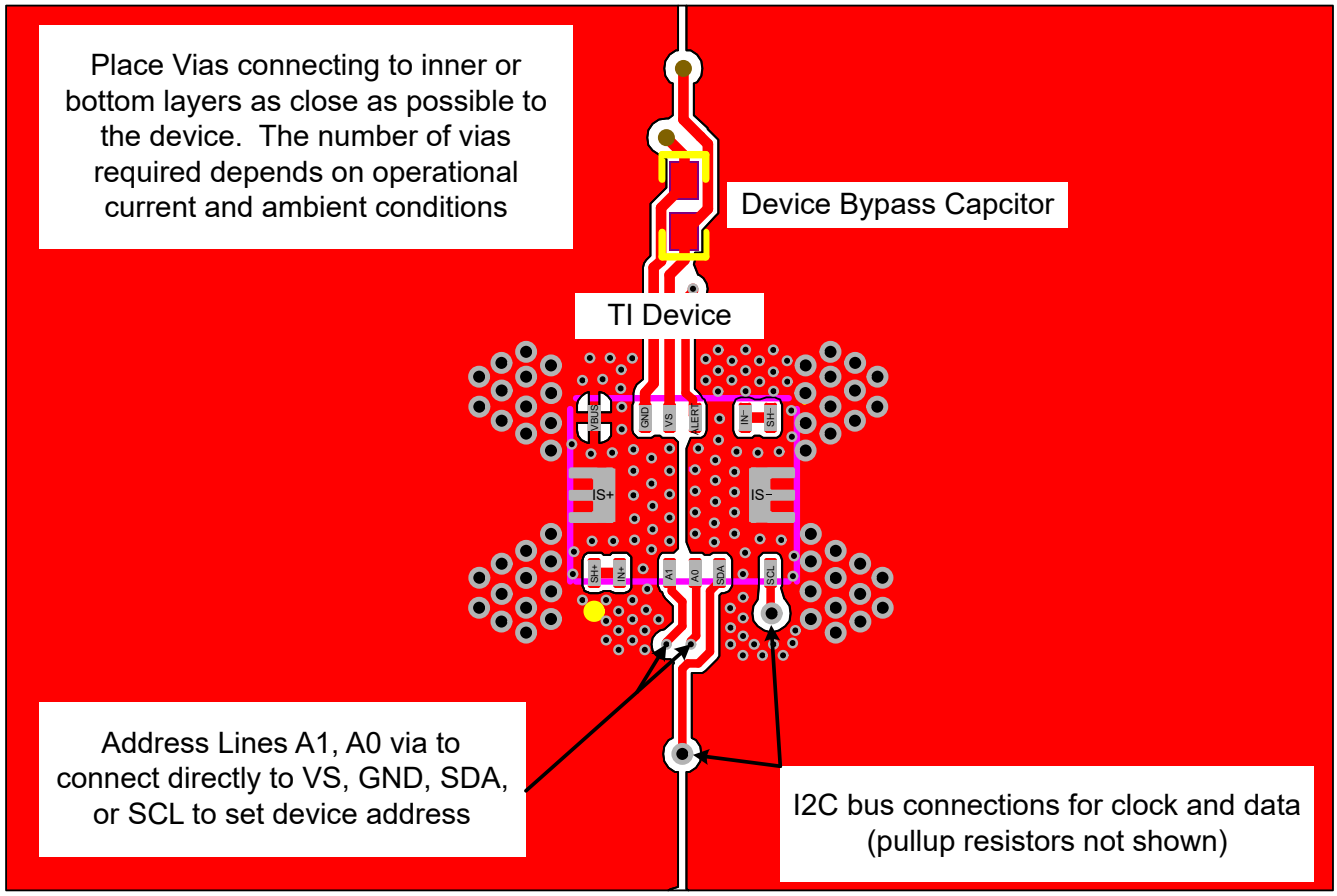
The input circuitry of the device can accurately measure signals on common-mode voltages beyond the power-supply voltage, V_S. For example, the voltage applied to the V_S power supply terminal can be 5 V, whereas the load power-supply voltage being monitored (the common-mode voltage) can be as high as 85 V. Note that the device can also withstand the full 0 V to 85 V range at the input terminals, regardless of whether the device has power applied or not. Avoid applications where the GND pin is disconnected while device is actively powered.

8.4 Layout

8.4.1 Layout Guidelines

Place the required power-supply bypass capacitors as close as possible to the supply and ground terminals of the device. A typical value for this supply bypass capacitor is 0.1 µF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

8.4.2 Layout Example



(1) All vias close to the pin pads should be tented.
(2) All Vias are either 8 mil/18 mil or 15 mil/25 mil with a 5 mill annular ring.
(3) The distance between the IS+ and IS- power pours is 8 mil.

図 8-3. INA741 Layout Example

ADVANCE INFORMATION

9 Device and Documentation Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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9.3 Trademarks

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9.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

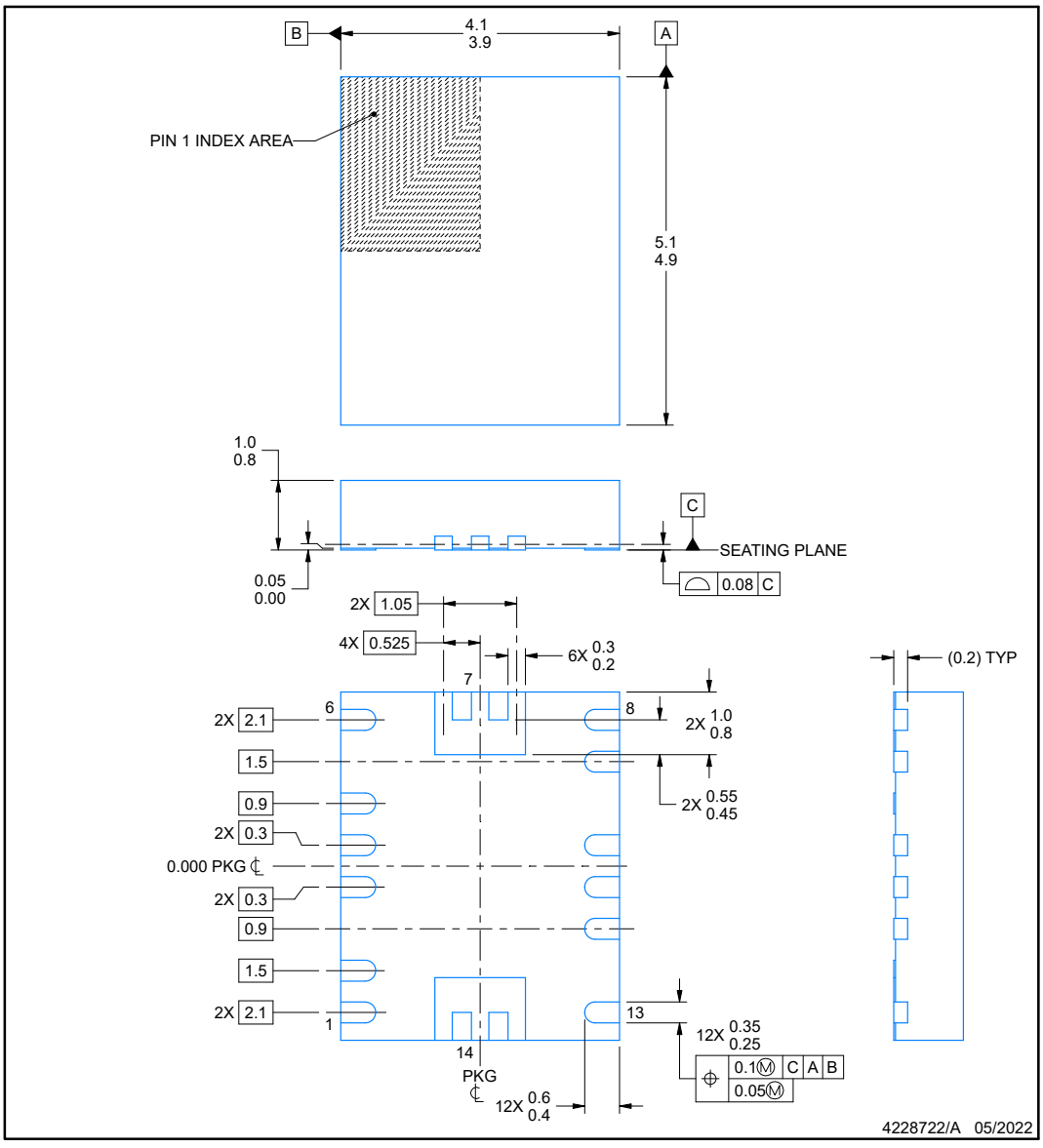
ADVANCE INFORMATION

PACKAGE OUTLINE

REM0014B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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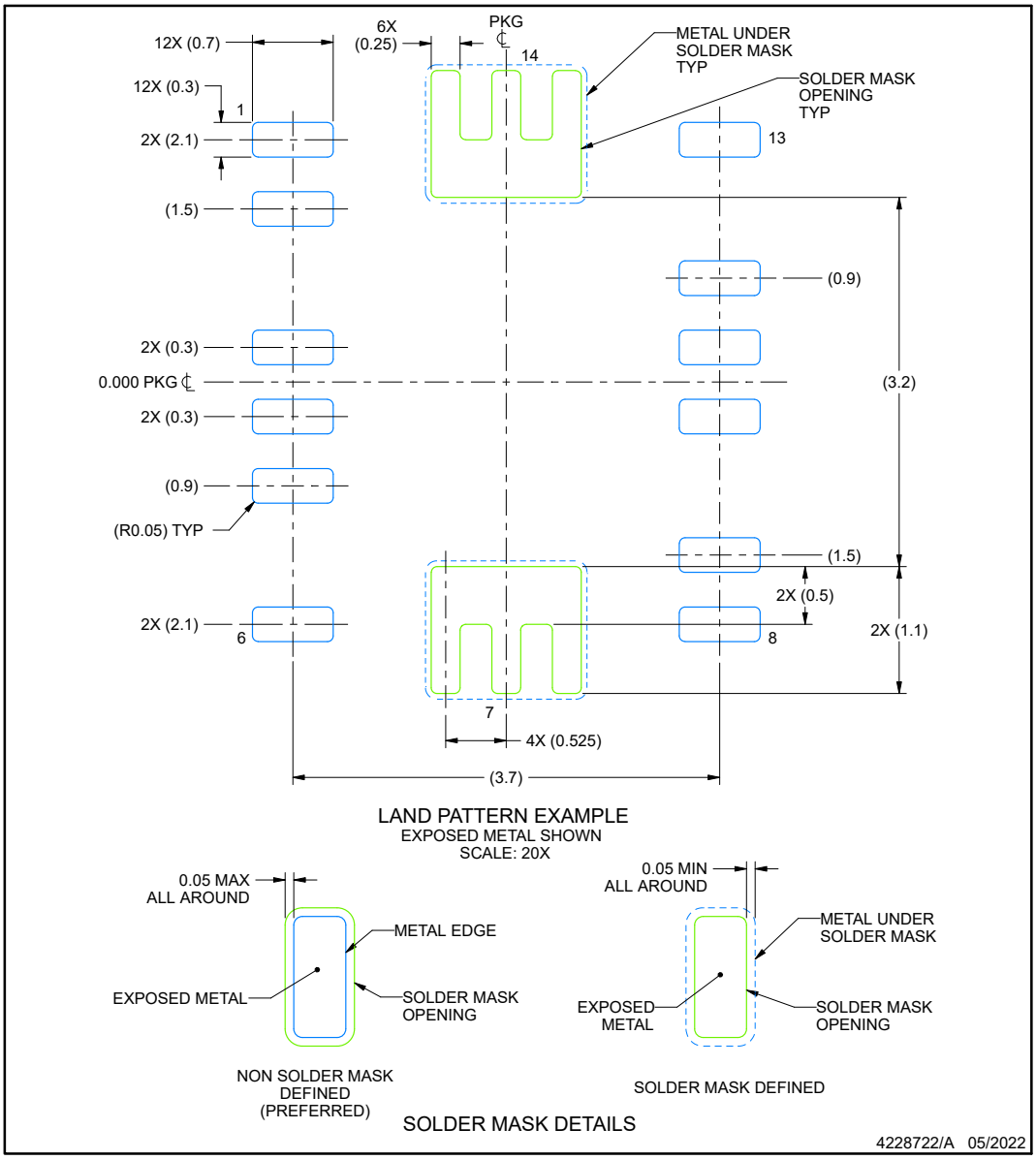
EXAMPLE BOARD LAYOUT

REM0014B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



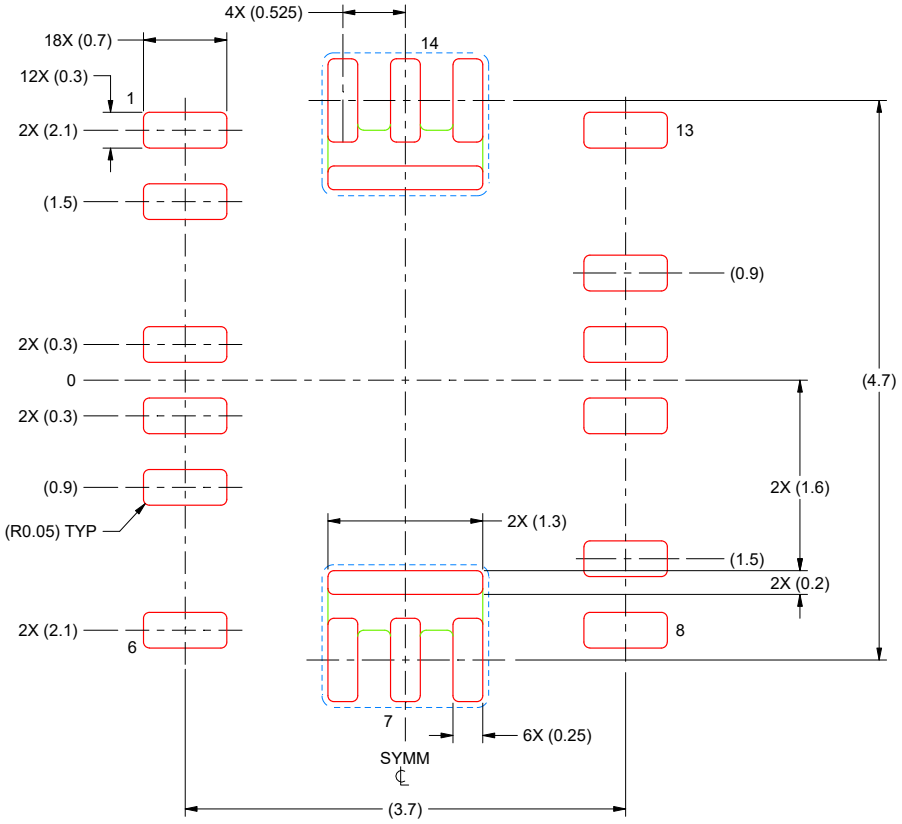
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

REM0014B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

4228722/A 05/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

10.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
PINA741AIREMR	ACTIVE	VQFN	REM	14	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PNA 741A

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

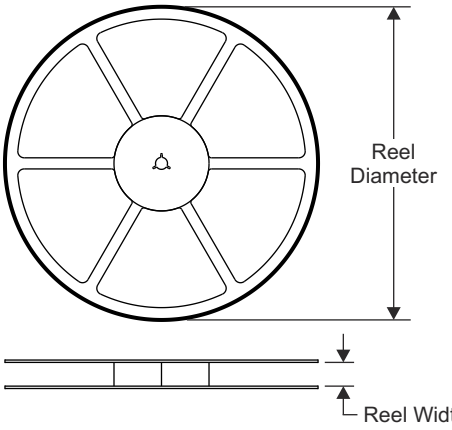
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

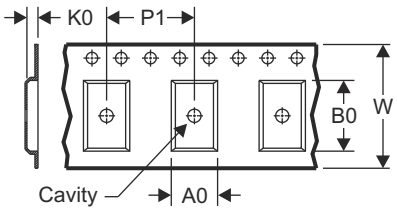
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

10.2 Tape and Reel Information

REEL DIMENSIONS

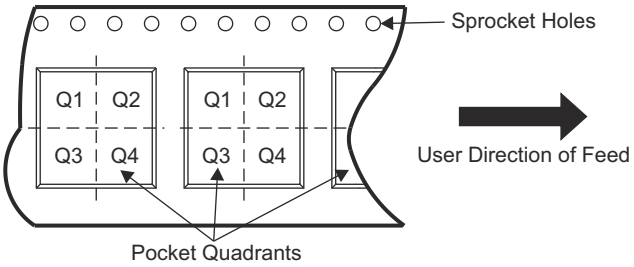


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PINA741AIREMR	VQFN	REM	14	5000	330	12.4	4.3	5.3	1.3	8	12	Q1

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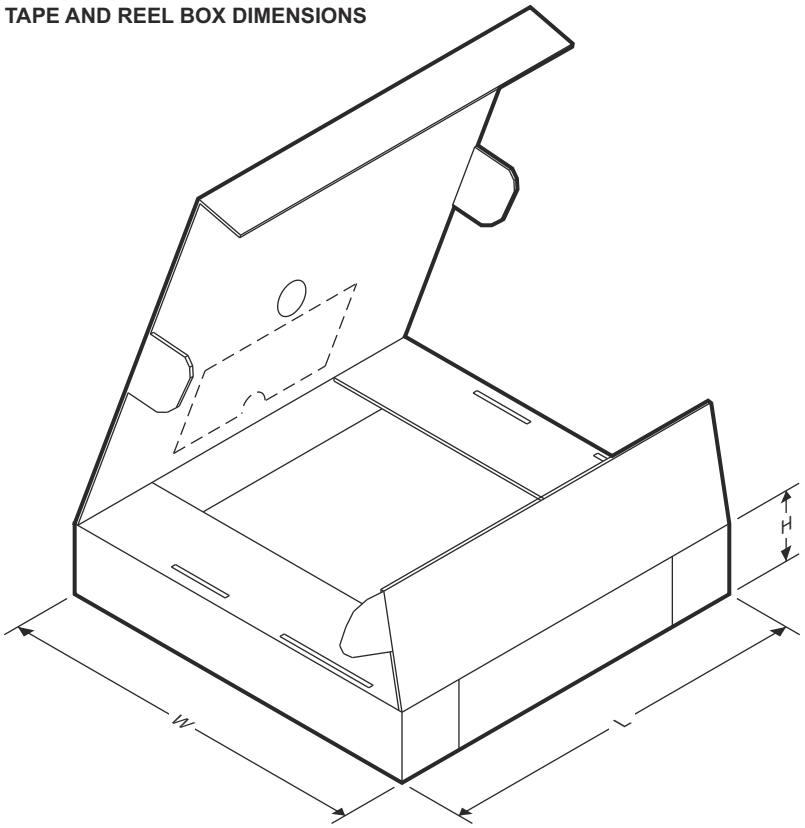
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PINA741AIREMR	VQFN	REM	14	5000	360	360	36

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PINA741AIREMR	ACTIVE	VQFN	REM	14	5000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

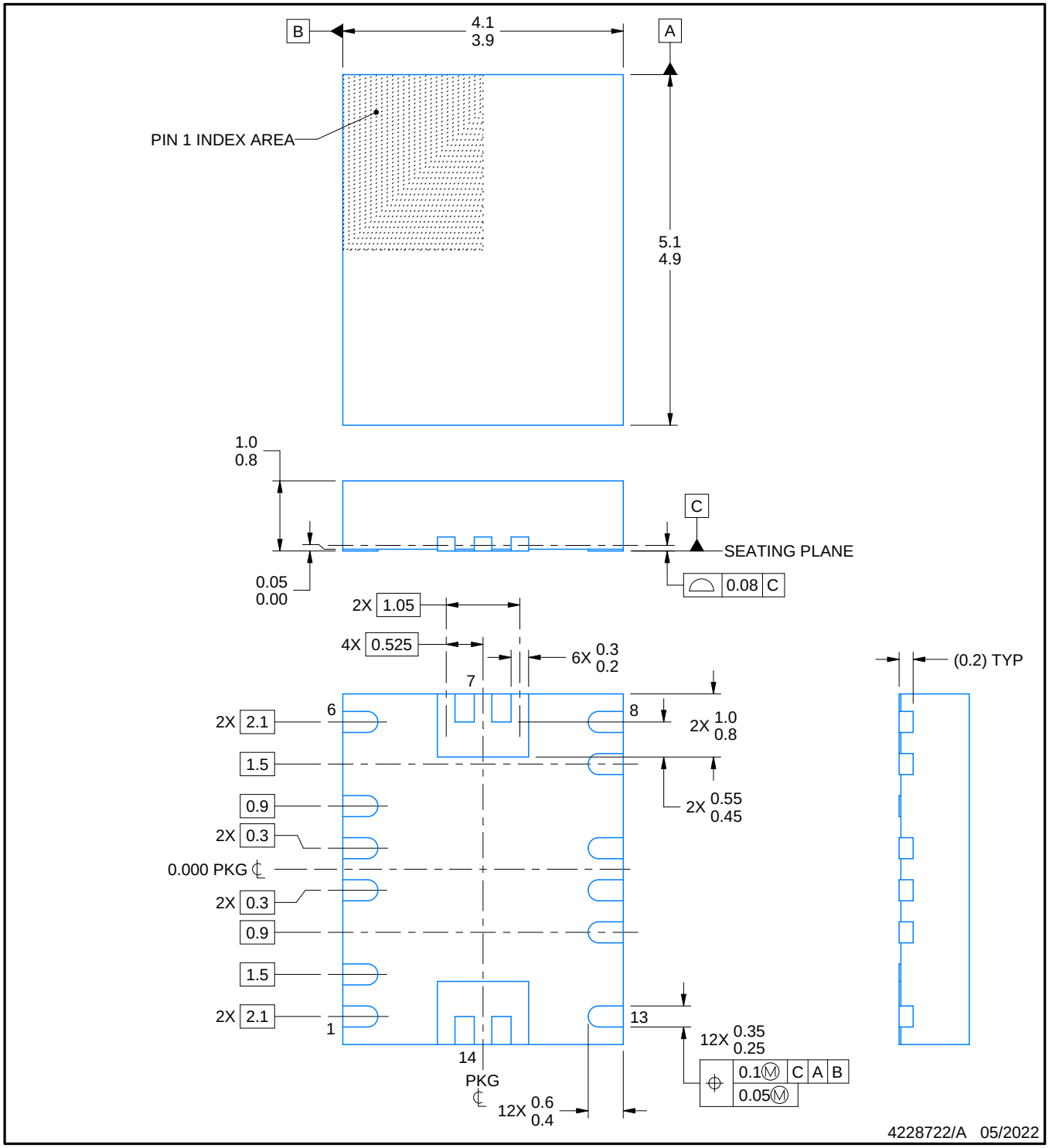
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

REM0014B

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

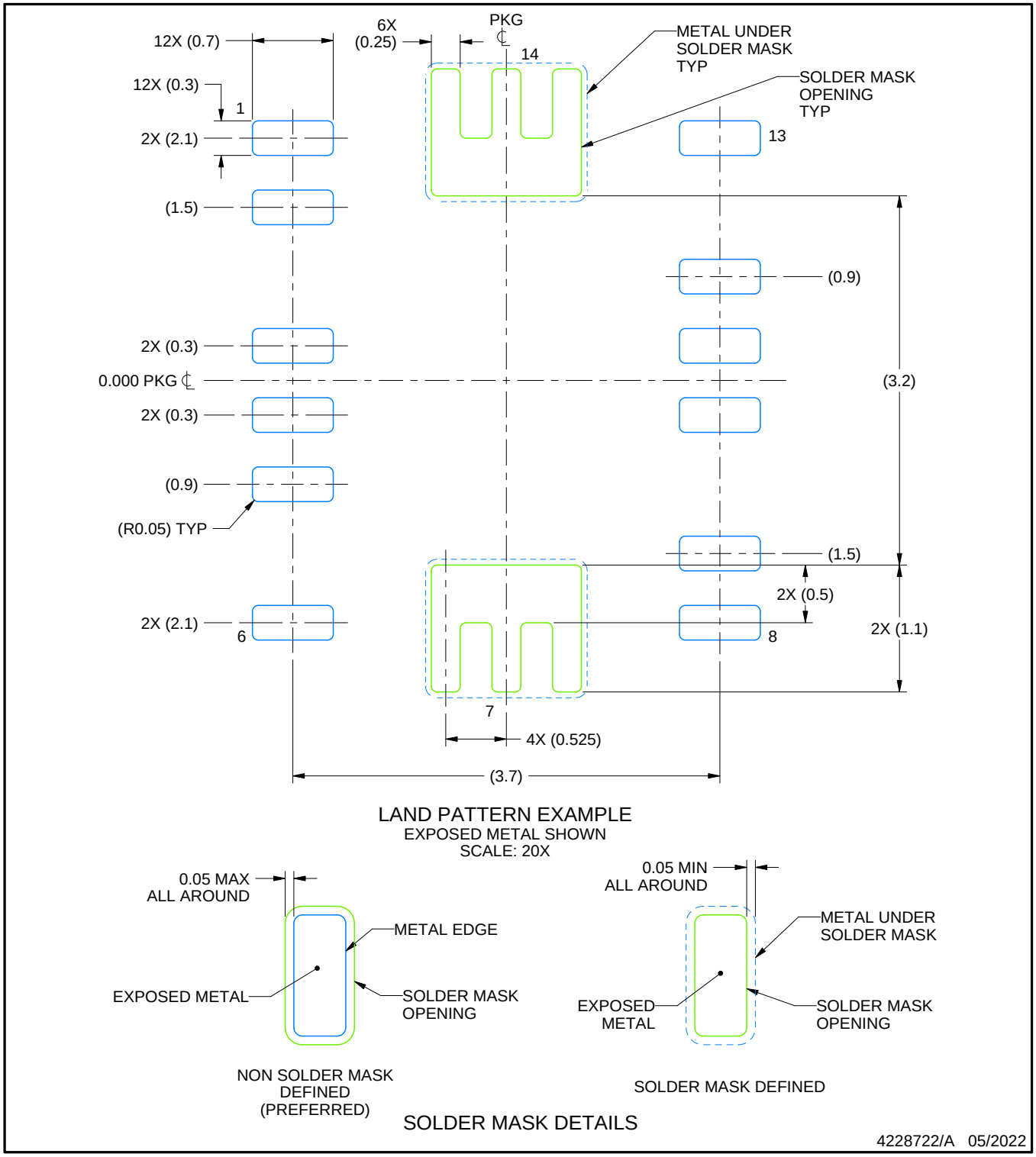
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

REM0014B

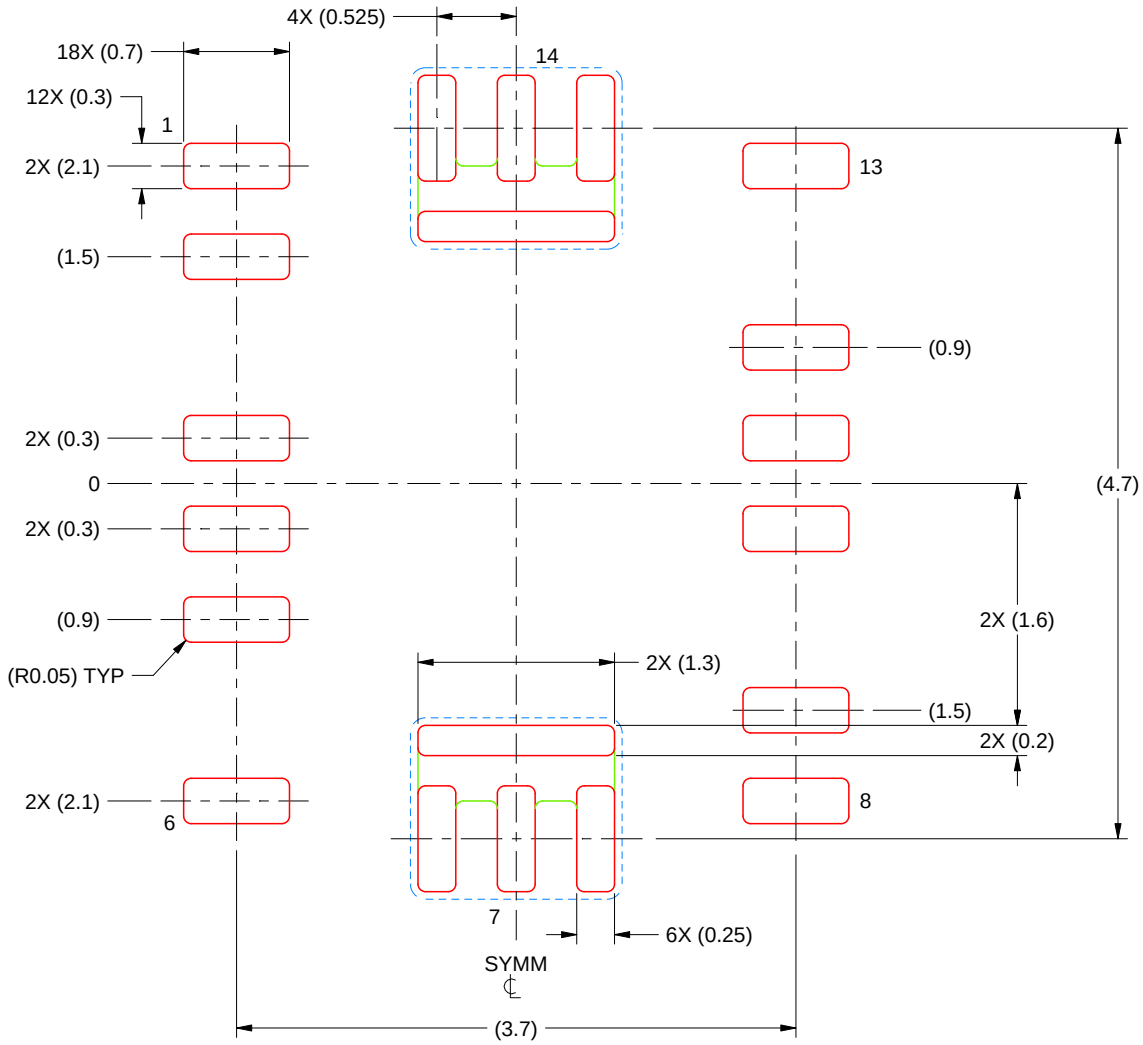
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

4228722/A 05/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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