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## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (November 2021) to Revision A (February 2022)	Page
• Updated C2 pin name to GPO/TS1 <a href="#">Pin Configurations and Functions</a> .....	3
• Updated <a href="#">Common Analog (LDO, LFO, HFO, REF1, REF2, I-WAKE)</a> .....	6
• Updated <a href="#">Gauge Measurements (ADC, CC, Temperature)</a> .....	11
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• Updated <a href="#">Typical Applications</a> .....	22
• Updated <a href="#">Layout Guidelines</a> .....	25

## 5 Pin Configurations and Functions

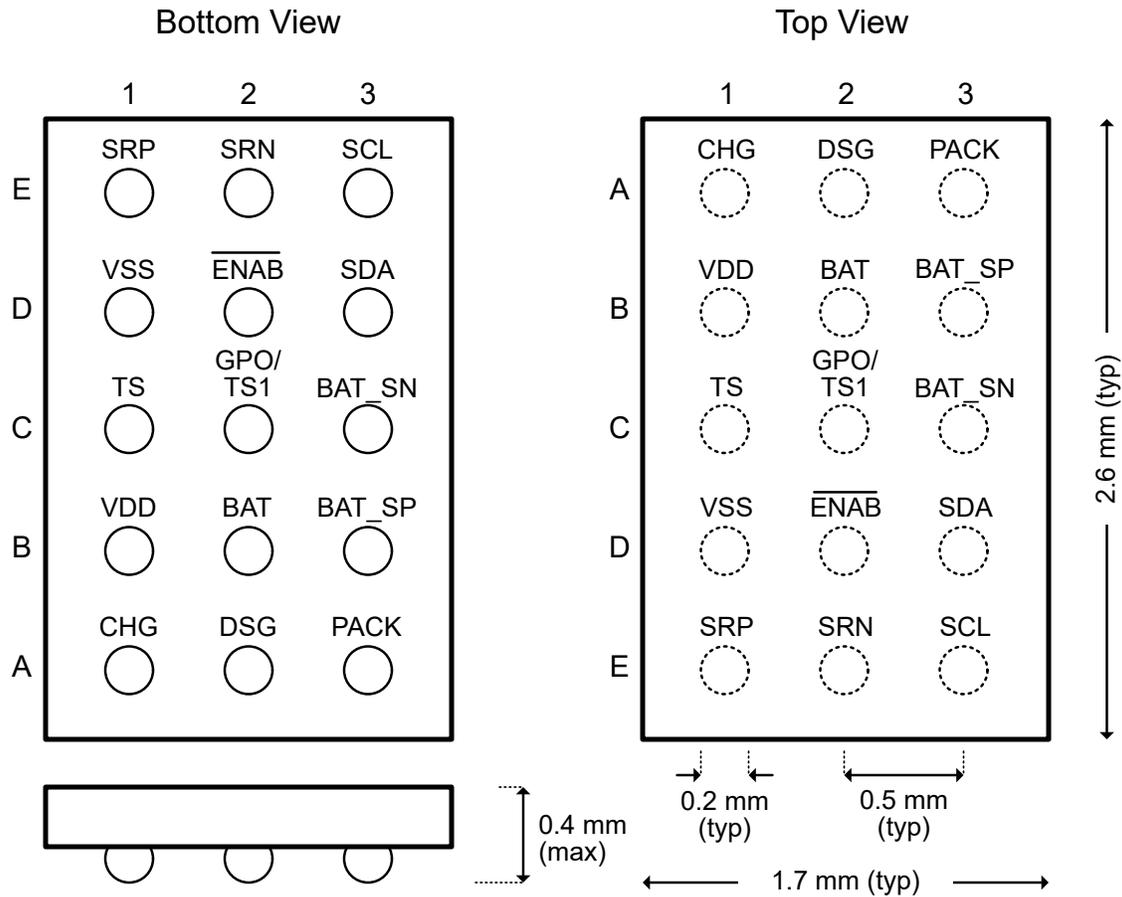


图 5-1. Pinout Diagram

表 5-1. Pin Functions

PIN			DESCRIPTION
NAME	NO.	TYPE <sup>(1)</sup>	
CHG	A1	AO	Charge FET (CHG) driver
DSG	A2	AO	Discharge FET (DSG) driver. Connect a series 10-M $\Omega$ typical resistor ( $R_{DSG}$ ) between DSG pin and PACK+ positive terminal.
PACK	A3	IA	Pack input voltage sensing pin. Connect a series 5-k $\Omega$ typical resistor ( $R_{PACK}$ ) between PACK pin and PACK+ positive terminal.
VDD	B1	P	LDO regulator input. Connect a 1- $\mu$ F typical capacitor ( $C_{VDD}$ ) between VDD and VSS. Place the capacitor close to the gauge.
BAT	B2	IA	Battery voltage measurement sense input
BAT_SP	B3	OA	Cell sense output, positive
BAT_SN	C3	OA	Cell sense output, negative
TS	C1	IA	Thermistor input to ADC with internal 18-k $\Omega$ pullup resistor
GPO/TS1	C2	I/O	General purpose output. Optional TS1 ADC input channel with internal 18-k $\Omega$ pullup resistor
VSS	D1	P	Device ground
ENAB	D2	I	Active low digital input with weak internal pullup to VDD. If enabled for ultra-low power SHIP mode, driving this signal to the PACK- negative terminal will enable the device to wake up.
SDA	D3	I/O	Digital input, open drain output for I <sup>2</sup> C serial data. Use with a typical 10-k $\Omega$ pullup resistor.
SCL	E3	I/O	Digital input, open drain output for I <sup>2</sup> C serial clock. Use with a typical 10-k $\Omega$ pullup resistor.

表 5-1. Pin Functions (continued)

PIN			DESCRIPTION
NAME	NO.	TYPE <sup>(1)</sup>	
SRP	E1	IA	This is the positive analog input pin connected to the internal coulomb-counter peripheral for integrating a small voltage between SRP (positive side) and SRN (negative side).
SRN	E2	IA	This is the negative analog input pin connected to the internal coulomb-counter peripheral for integrating a small voltage between SRP (positive side) and SRN (negative side).

(1) I/O = Digital input/output, IA = Analog input, AO= Analog output, P = Power connection

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage range	VDD	-0.3	6	V
Input voltage range	PACK (limited to 4 mA max)	-0.3	8	V
	PACK+ external battery pack input terminal with 5 kΩ resistor in series to device PACK input pin	-0.3	24	
	PACK+ external battery pack input terminal with a 5 kΩ resistor (R <sub>PACK</sub> ) in series to device PACK pin and a 10 MΩ resistor (R <sub>DSG</sub> ) to device DSG pin	-12	24	
	BAT	-0.3	6	
	SDA, SCL, ENAB	-0.3	6	
	TS	-0.3	2	
	SRP, SRN	-0.3	V <sub>BAT</sub> + 0.3	
Output voltage range	BAT_SP, BAT_SN	-0.3	6	V
	CHG, DSG	-0.3	12	
Operating junction temperature, T <sub>J</sub>		-40	85	°C
Storage temperature, T <sub>stg</sub>		-65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM) on all pins, per ANSI/ESDA/ JEDEC JS-001 <sup>(1)</sup>	V
		Charged-device model (CDM) on all pins, per ANSI/ESDA/ JEDEC JS-002 <sup>(2)</sup>	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage range	VDD	2.0		5.5	V

### 6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage range	PACK (with 5 kΩ R <sub>PACK</sub> current limit)	0		12	V
	PACK (no R <sub>PACK</sub> current limit)	0		5.5	
	BAT	1.5		5.5	
	SDA, SCL, ENAB	–0.3		VDD	
	TS	VSS		1.8	
	SRN, SRP	V <sub>CC_CM</sub> – 0.1		V <sub>CC_CM</sub> + 0.1	
Output voltage range	BAT_SP, BAT_SN	2		VDD + V <sub>OFFS</sub>	V
	GPO	VSS		1.8	
	CHG, DSG	VSS		VDD+ (VDD × A <sub>FETON</sub> )	
External Decoupling Capacitor on VDD pin, C <sub>VDD</sub>		1			μF
External Decoupling Capacitor on TS pin, C <sub>TS</sub>				0.01	μF
External Sense Resistor from PACK+ terminal to device PACK pin, R <sub>PACK</sub>		5			kΩ
External Sense Resistor from PACK+ terminal to device DSG pin, R <sub>DSG</sub>		10			MΩ
External Sense Resistor from SRN to SRP pins, R <sub>SNS</sub>		1		20	mΩ
Operating Temperature, T <sub>A</sub>		–40		85	°C

### 6.4 Thermal Information

Over-operating free-air temperature range (unless otherwise noted)

THERMAL METRIC <sup>(1)</sup>		YAH (DSBGA)	UNIT
		(15 PINS)	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	70	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	17	
R <sub>θJB</sub>	Junction-to-board thermal resistance	20	
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	1	
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	18	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	NA	

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

### 6.5 Electrical Characteristics

#### 6.5.1 Supply Current

Unless otherwise noted, characteristics noted under conditions of T<sub>A</sub> = –40 to 85°C, no host communications, PROT On<sup>(1)</sup>, V<sub>CHG</sub> and V<sub>DSG</sub> > 5 V, C<sub>LOAD</sub> = 8 nF (typical 20 nA), VDD = 4 V, Average current over 30 s with default firmware settings

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>NORMAL</sub>	Standard operating conditions		57		μA
I <sub>SLEEP</sub>	Measured current ≤ sleep current threshold		20		μA
I <sub>SHIP</sub>	V <sub>BAT</sub> = 3.0 V, Firmware SHIP mode enabled. 60 s average		10		μA
I <sub>SHELF</sub>	V <sub>BAT</sub> = 3.0 V, Firmware SHELF mode enabled. PROT Off. 60 s average		5		μA

### 6.5.1 Supply Current (continued)

Unless otherwise noted, characteristics noted under conditions of  $T_A = -40$  to  $85^\circ\text{C}$ , no host communications, PROT On<sup>(1)</sup>,  $V_{\text{CHG}}$  and  $V_{\text{DSG}} > 5\text{ V}$ ,  $C_{\text{LOAD}} = 8\text{ nF}$  (typical 20 nA),  $V_{\text{DD}} = 4\text{ V}$ , Average current over 30 s with default firmware settings

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{\text{SHUT}}$	Firmware SHUTDOWN mode enabled OR $V_{\text{BAT}} \leq V_{\text{SHUT}}$ , PROT Off		0.2	1	$\mu\text{A}$

(1) PROT On/Off. Protector block enabled with both DSG and CHG pins On or Off.

### 6.5.2 Common Analog (LDO, LFO, HFO, REF1, REF2, I-WAKE)

Unless otherwise noted, characteristics noted under conditions of  $T_A = -40$  to  $85^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Internal 1.8-V LDO (REG18)</b>					
$V_{\text{REG18}}$	Regulator output voltage	1.6	1.8	2.0	V
$\Delta V_{\text{REG18TEMP}}$	Regulator output change with temperature	$\Delta V_{\text{BAT}}/\Delta T_A$ , $I_{\text{REG18}} = 10\text{ mA}$		+1.2%	
$\Delta V_{\text{REG18LINE}}$	Line regulation	-0.8%		0.8%	
$\Delta V_{\text{REG18LOAD}}$	Load regulation	$I_{\text{REG18}} = 16\text{ mA}$		1.5%	
$I_{\text{SHORT}}$	Short Circuit Current Limit	$V_{\text{REG18}} = 0\text{ V}$		60	mA
$\text{PSRR}_{\text{REG18}}$	Power Supply Rejection Ratio	$\Delta V_{\text{BAT}}/\Delta V_{\text{REG18}}$ , $I_{\text{REG18}} = 10\text{ mA}$ , $V_{\text{BAT}} > 2.5\text{ V}$ , $f = 10\text{ Hz}$		50	dB
$V_{\text{PORth}}$	POR threshold	Rising Threshold		1.75	V
$V_{\text{PORhy}}$	POR hysteresis		0.1		V
$V_{\text{ENAB}}$	$\overline{\text{ENAB}}$ turn-on voltage for LDO <sup>(1)</sup>	Active low falling threshold		0.4	V
$R_{\text{ENAB}}$	$\overline{\text{ENAB}}$ pin pullup resistance <sup>(1)</sup>	Internal pull-up to VDD		1.3	M $\Omega$
<b>Low Frequency Internal Oscillator (LFO)</b>					
$f_{\text{LFO}}$	LFO Operating frequency	Normal operating mode		65.536	kHz
$f_{\text{LFO(ERR)}}$	LFO Frequency error	-2.5%		+2.5%	
$f_{\text{LFO32}}$	LFO operating frequency	Low power mode		32.768	kHz
$f_{\text{LFO32(ERR)}}$	LFO frequency error	-5%		+5%	
<b>High Frequency Internal Oscillator (HFO)</b>					
$f_{\text{HFO}}$	HFO operating frequency		16.78		MHz
$f_{\text{HFO(ERR)}}$	HFO frequency error	$T_A = -20^\circ\text{C}$ to $70^\circ\text{C}$		2.5%	
		$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		3.5%	
$t_{\text{HFOSTART}}$	HFO start-up time	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ , CLKCTL[HFRAMP] = 1, oscillator frequency within +/- 3% of nominal frequency or a power-on reset		4	ms
<b>Voltage Reference1 (VREF1)</b>					
$V_{\text{REF1}}$	Internal reference voltage	REF1 is for protection circuits, LDO, and CC		1.227	V
$V_{\text{REF1\_DRIFT}}$	Internal Reference Voltage Drift	-80		+80	PPM/ $^\circ\text{C}$
<b>Voltage Reference2 (VREF2)</b>					
$V_{\text{REF2}}$	Internal Reference Voltage	REF2 is for the ADC		1.22	V
$V_{\text{REF2\_DRIFT}}$	Internal Reference Voltage Drift	-20		+20	PPM/ $^\circ\text{C}$
<b>Wake-Up Comparator (I-WAKE)</b>					
$V_{\text{WAKE}}$	Sense resistor voltage threshold range to wake-up gauge from low-power states <sup>(2)</sup>	500 $\mu\text{V}$ step. Data Flash firmware default is 2 mV typical		-2.5	mV

### 6.5.2 Common Analog (LDO, LFO, HFO, REF1, REF2, I-WAKE) (continued)

Unless otherwise noted, characteristics noted under conditions of  $T_A = -40$  to  $85^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{\text{WAKE}}$	Effective wake-up current threshold range	Ideal $R_{\text{SNS}} = 1\text{ m}\Omega$	-1000		-3000	mA
		Ideal $R_{\text{SNS}} = 2\text{ m}\Omega$	-500		-1500	
		Ideal $R_{\text{SNS}} = 5\text{ m}\Omega$	-200		-600	
$V_{\text{WAKE\_ACC}}$	Wake-up detection accuracy (2)		-250		250	$\mu\text{V}$
$t_{\text{WAKE}}$	I-WAKE detection delay options (1)	Configurable with two delay options. Data Flash firmware default is 12 ms typical	9.6	12	14.4	ms
			19.2	24	28.8	

(1) Specified by design

(2) Data flash is configurable in FULL ACCESS mode and locked in SEALED. Accuracy is assured by factory trim at specified default threshold. A change in the factory threshold requires device calibration in the field.

### 6.5.3 Battery Protection (CHG, DSG)

Protection hardware circuits operating over free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>N-CH FET DRIVER, CHG AND DSG</b>						
$V_{\text{DRIVER}}$	Gate Driver Voltage, $V_{\text{CHG}}$ or $V_{\text{DSG}}$	$C_{\text{LOAD}} = 8\text{ nF}$	$2 \times V_{\text{DD}}$			V
$A_{\text{FETON}}$	FET driver gain factor, Vgs voltage to FET	$A_{\text{FETON}} = (V_{\text{driver}} - V_{\text{DD}})/V_{\text{DD}}$ , $C_{\text{LOAD}} = 8\text{ nF}$ , $UVP < V_{\text{DD}} < 3.8\text{ V}$	0.9	1.0	1.2	V/V
$V_{\text{DSGOFF}}$	DSG FET driver off output voltage	$V_{\text{DSGOFF}} = V_{\text{DSG}} - \text{PACK}$ , $C_L = 8\text{ nF}$			0.2	V
$V_{\text{CHGOFF}}$	CHG FET driver off output voltage	$V_{\text{CHGOFF}} = V_{\text{CHG}} - V_{\text{SS}}$ , $C_L = 8\text{ nF}$			0.2	V
$t_{\text{rise}}$	FET driver rise time (1)	$C_L = 8\text{ nF}$ , $(V_{\text{driver}} - V_{\text{DD}})/V_{\text{DD}} = 1 \times V_{\text{FETON}}$ changes from VDD to $2 \times V_{\text{DD}}$		400	800	us
$t_{\text{fall}}$	FET driver fall time (1)	$C_L = 8\text{ nF}$ , $V_{\text{FETON}}$ changes from $V_{\text{FETMAX}}$ to $V_{\text{FETOFF}}$		50	200	us
$V_{\text{FET\_SHUT}}$	Firmware FET driver shut down voltage (2) (4)	Configurable with 1-mV steps	2000	2100	5000	mV
$V_{\text{FET\_SHUT\_REL}}$	Firmware FET driver shut down release (2) (4)		2000	2300	5000	
$I_{\text{LOAD}}$	FET driver maximum loading				10	$\mu\text{A}$
<b>VOLTAGE PROTECTION</b>						
$V_{\text{OVP}}$	Hardware overvoltage protection (OVP) detection range (3)	Recommended threshold range.	3500		5000	mV
	Factory default trimmed threshold(3)	Factory trimmed in 50-mV steps	4525			
$V_{\text{OVP\_ACC}}$	Hardware OVP detection accuracy (3)	$T_A = 25^\circ\text{C}$ , $C_{\text{LOAD}}$ at CHG/DSG $< 1\text{ }\mu\text{A}$	-15		15	mV
		$T_A = 0^\circ\text{C}$ to $60^\circ\text{C}$ , $C_{\text{LOAD}}$ at CHG/DSG $< 1\text{ }\mu\text{A}$	-25		25	mV
		$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ , $C_{\text{LOAD}}$ at CHG/DSG $< 1\text{ }\mu\text{A}$	-50		50	mV
$V_{\text{FW\_OVP}}$	Firmware OVP detection range (4)	Configurable with 1-mV steps	2000	4490	5000	mV
$V_{\text{FW\_OVP\_REL}}$	Firmware OVP release range (4)		2000	4290	5000	mV
$V_{\text{UVP}}$	Hardware undervoltage (UVP) detection range (3)	Recommended threshold range.	2000		4000	mV
	Factory default trimmed threshold(3)	Factory trimmed in 50-mV steps	2300			

### 6.5.3 Battery Protection (CHG, DSG) (continued)

Protection hardware circuits operating over free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>UVP_ACC</sub>	Hardware UVP detection accuracy <sup>(3)</sup>	TA = 25°C, C <sub>LOAD</sub> at CHG/DSG < 1 μA	-20		20	mV
		TA = 0°C to 60°C, C <sub>LOAD</sub> at CHG/DSG < 1μA	-30		30	mV
		TA = -40°C to 85°C, C <sub>LOAD</sub> at CHG/DSG < 1μA	-50		50	mV
V <sub>FW_UVP</sub>	Firmware UVP detection range <sup>(4)</sup>	Configurable with 1 mV steps	2000	2500	5000	
V <sub>FW_UVP_REL</sub>	Firmware UVP release range <sup>(4)</sup>		2000	2900	5000	mV
R <sub>PACK-VSS</sub>	Resistance between PACK and VSS	SHUTDOWN mode only	100	300	550	kΩ
V <sub>RCP</sub>	Reverse Charge Protection limit	-10V Continuous Operating, -12 V ABS MAX	-10			V
<b>CURRENT PROTECTION</b>						
V <sub>OCC</sub>	Sense voltage threshold range for Overcurrent in Charge (OCC) <sup>(3) (4)</sup>	Recommended threshold range.	1		100	mV
	Factory default trimmed threshold <sup>(3)</sup>	Factory trimmed in 1-mV steps		14		
V <sub>OCC</sub>	OCC 2-mV step design option	2 mV step configuration option	2		256	mV
I <sub>OCC</sub>	Effective OCC current threshold range from V <sub>OCC</sub> <sup>(1) (4)</sup>	Ideal R <sub>SNS</sub> = 1 mΩ	4	14	100	A
		Ideal R <sub>SNS</sub> = 2 mΩ	2	7	50	
		Ideal R <sub>SNS</sub> = 5 mΩ	0.8	2.8	20	
I <sub>FW_OCC</sub>	Firmware OCC detection range <sup>(4)</sup>	Configurable with 1 mA steps	0	12000	+I <sub>CC_IN</sub>	mA
V <sub>OCD</sub>	Sense voltage threshold range for Overcurrent in discharge (OCD) <sup>(3) (4)</sup>	Recommended threshold range.	-4		-100	mV
	Factory default trimmed threshold <sup>(3)</sup>	Factory trimmed in 1-mV steps		-16		
V <sub>OCD</sub>	OCD 2-mV step design option	±2 mV step configuration option	-2		-256	mV
I <sub>OCD</sub>	Effective OCD current threshold range from V <sub>OCD</sub> <sup>(1) (4)</sup>	Ideal R <sub>SNS</sub> = 1 mΩ	-4	-16	-100	A
		Ideal R <sub>SNS</sub> = 2 mΩ	-2	-8	-50	
		Ideal R <sub>SNS</sub> = 5 mΩ	-0.8	-3.2	-20	
I <sub>FW_OCD</sub>	Firmware OCD detection range <sup>(4)</sup>	Configurable with 1-mA steps	-I <sub>CC_IN</sub>	-7000	0	mA
V <sub>SCD</sub>	Sense voltage threshold range for Short circuit current in discharge (SCD) <sup>(3) (4)</sup>	Threshold factory trimmed with 1-mV steps	-5		-120	mV
	Factory default trimmed threshold <sup>(3)</sup>			-20		
I <sub>SCD</sub>	Effective SCD current threshold range from V <sub>SCD</sub> <sup>(1) (4)</sup>	Ideal R <sub>SNS</sub> = 1 mΩ	-5	-20	-120	A
		Ideal R <sub>SNS</sub> = 2 mΩ	-2.5	-10	-60	
		Ideal R <sub>SNS</sub> = 5 mΩ	-1	-4	-24	
V <sub>OC_ACC</sub>	Overcurrent (OCC, OCD, SCD) detection accuracy <sup>(3)</sup>	<20 mV, TA = -25°C to 60°C	-2.1		2.1	mV
		<20 mV	-2.1		2.1	
		20 mV–55 mV	-3		3	
		56 mV–100 mV	-5		5	
		>100 mV	-12		12	
I <sub>PACK-VDD</sub>	Current sink between PACK and VDD during current fault	Load removal detection in firmware		15		μA
V <sub>OC_REL</sub>	OCC fault release threshold	(V <sub>PACK</sub> - V <sub>BAT</sub> )		100		mV
	OCD, SCD fault release threshold			-400		mV
<b>OVERTEMPERATURE PROTECTION</b>						

### 6.5.3 Battery Protection (CHG, DSG) (continued)

Protection hardware circuits operating over free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T <sub>OTC_TRIP</sub>	OTC trip/release threshold (2) (4)	Firmware-based and configurable in 0.1°C steps	-40.0	55.0	150.0	°C
T <sub>OTC_REL</sub>			-40.0	50.0	150.0	°C
T <sub>OTD_TRIP</sub>	OTD trip/release threshold (2) (4)		-40.0	60.0	150.0	°C
T <sub>OTD_REL</sub>			-40.0	55.0	150.0	°C
T <sub>UTC_TRIP</sub>	UTC trip/release threshold (2) (4)		-40.0	0.0	150.0	°C
T <sub>UTC_REL</sub>			-40.0	5.0	150.0	°C
T <sub>UTD_TRIP</sub>	UTD trip/release threshold (2) (4)		-40.0	0.0	150.0	°C
T <sub>UTD_REL</sub>			-40.0	5.0	150.0	°C
<b>PROTECTION DELAY<sup>(1)</sup></b>						
t <sub>OVP</sub>	OVP detection delay (debounce) options (1) (4)	Configurable with 4095 delay options in 1.953-ms steps. Factory default = 1000 ms (512 counts) typical	1.953	1000	7998	ms
t <sub>UVP</sub>	UVP detection delay (debounce) options (1) (4)	Configurable with 127-delay options in 1.953-ms steps. Factory default = 127 ms (65 counts) typical	1.953	127	248	ms
t <sub>OCD</sub>	OCD detection delay (debounce) options (1) (4)	Configurable with 31 delay options in 1.953-ms steps. Factory default = 7.8 ms (4 counts) typical	1.953	7.8	60.5	ms
t <sub>OCC</sub>	OCC detection delay (debounce) options (1) (4)	Configurable with 255 delay options in 0.244-ms steps. Factory default = 15.9 ms (65 counts) typical	0.244	15.9	62.3	ms
t <sub>SCD</sub>	SCD detection delay (debounce) options (1) (4)	Configurable with seven delay options in 122-μs steps. Factory default = 244-μs (2 counts) typical	122	244	854	μs
T <sub>OTC_DLY</sub>	OTC trip delay <sup>(2) (4)</sup>	Firmware-based and configurable in 1-s steps. The typical value is the data flash factory default.	0	2	255	s
T <sub>OTD_DLY</sub>	OTD trip delay <sup>(2) (4)</sup>		0	2	255	s
T <sub>UTC_DLY</sub>	UTC trip delay <sup>(2) (4)</sup>		0	2	255	s
T <sub>UTD_DLY</sub>	UTD trip delay <sup>(2) (4)</sup>		0	2	255	s
<b>ZERO VOLT (LOW VOLTAGE) CHARGING</b>						
V <sub>0CHGR</sub>	Charger voltage requires to start zero-volt charging	V <sub>PACK</sub> – V <sub>SS</sub>	1.6			V
V <sub>0INH</sub>	Battery voltage that inhibits zero-volt charging	V <sub>DD</sub> – V <sub>SS</sub>		1.0	1.1	V

- (1) Specified by design. Not production tested.
- (2) Firmware-based parameter. Not production tested.
- (3) Accuracy assured by factory trim at specified default threshold. A change from the default threshold requires device calibration in the field. Refer to the [BQ27Z746 Technical Reference Manual](#).
- (4) Specified typical value is the factory default. Not production tested. The data flash configuration value can be changed in FULL ACCESS mode and is locked in SEALED mode. Refer to the [BQ27Z746 Technical Reference Manual](#).

### 6.5.4 Cell Sensing Output (BAT\_SP, BAT\_SN)

Unless otherwise noted, characteristics noted under conditions of T<sub>A</sub> = –40 to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Static Response</b>						
V <sub>BUFACC</sub>	Buffer accuracy (BAT_SP – BAT_SN)	V <sub>BAT</sub> @ 1500 mV and 2400 mV DC, PACK-BAT_SP ≥ 200 mV, BAT_SP load: Hi-Z to 1 kΩ, BAT_SN load: 1 kΩ to 10 kΩ	1450	1500	1550	mV
			2350	2400	2450	

### 6.5.4 Cell Sensing Output (BAT\_SP, BAT\_SN) (continued)

Unless otherwise noted, characteristics noted under conditions of  $T_A = -40$  to  $85^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{\text{BUFOFFS}}$	BAT_SN common mode shift (BAT_SN – VSS)	400-mV option, $V_{\text{BAT}} = 1.5$ V to 2.5 V	370	400	430	mV
		200-mV option, $V_{\text{BAT}} = 2.0$ V to 2.5 V	170	200	230	
		0-mV option, $V_{\text{BAT}} = 2.0$ V to 2.5 V	–30	0	30	
		600-mV option, $V_{\text{BAT}} = 2.0$ to 2.5 V	550	600	650	
$\Delta V_{\text{BUF\_LINE}}$	Buffer line regulation	$V_{\text{BAT}} = 1.5$ to 2.5 V, no load, BAT_SP – BAT_SN, $V_{\text{PACK}} - V_{\text{BAT}} = 1.0$ V		10		mV
$\Delta V_{\text{BUF\_LOAD}}$	Buffer load regulation	$V_{\text{BAT}} = 2.4$ V, load = 1 mA, BAT_SP – BAT_SN, $V_{\text{PACK}} - V_{\text{BAT}} = 1.0$ V		1.2		mV
$V_{\text{RLOACC}}$	RLO mode accuracy (BAT_SP – BAT_SN)	$V_{\text{BAT}} = 3000$ -mV to 5000-mV DC, For stability, 0-mV buffer option enabled BAT_SP load: Hi-Z to 1 k $\Omega$ BAT_SN load: 1 k $\Omega$ to 10 k $\Omega$	–7		+7	mV
$V_{\text{RLOACP}}$	RLO mode accuracy (BAT_SP – VSS)		–5		+5	
$V_{\text{RLOACCN}}$	RLO mode accuracy (BAT_SN – VSS)		–5		+5	
$R_{\text{LO\_SP}}$	BAT_SP low resistance mode	200- $\Omega$ option, DSG FET = ON	160	200	260	$\Omega$
		510- $\Omega$ option, DSG FET = ON	459	510	561	
$R_{\text{LO\_SN}}$	BAT_SN low resistance mode	200- $\Omega$ option, DSG FET = ON	160	200	260	$\Omega$
		510- $\Omega$ option, DSG FET = ON	459	510	561	
$R_{\text{HIZ\_SP}}$	BAT_SP high impedance mode	CHG FET = OFF	0.6	1.0	1.3	M $\Omega$
$R_{\text{HIZ\_SN}}$	BAT_SN high impedance mode		0.6	1.0	1.3	
$t_{\text{BUF\_OFF}}$	Buffer turn-off timing <sup>(1)</sup>	Buffer disable timing respect to DSG FET turn-on		500		us
$C_{\text{BUF\_SP}}$	Max external capacitance for stable operation <sup>(1)</sup>	BAT_SP to SRN (PACK–)			150	pF
$C_{\text{BUF\_SN}}$		BAT_SN to SRN (PACK–)			150	
$B_{\text{BUF\_BW}}$	Buffer unity gain bandwidth <sup>(1)</sup>	Buffer enabled		30		kHz
$V_{\text{BCP}}$	BAT_SP – BAT +Fault (BCP) Threshold Range <sup>(1)</sup>	Recommended threshold range. Factory trimmed in $\approx 2$ -mV steps	+100		+250	mV
	Factory default trimmed threshold <sup>(3)</sup>			+200		
$V_{\text{BCP\_ACC}}$	BAT_SP – BAT +Fault Accuracy <sup>(3)</sup>	RLO mode enabled, Step size 10 mV	–10		+10	
$V_{\text{BDP}}$	BAT_SP – BAT –Fault (BDP) Threshold Range <sup>(1)</sup>	Recommended threshold range. Factory trimmed in $\approx 2$ -mV steps	–250		–100	mV
	Factory default trimmed threshold <sup>(3)</sup>			–200		
$V_{\text{BDP\_ACC}}$	BAT_SP – BAT –Fault Accuracy <sup>(3)</sup>	RLO mode enabled, Step size 10 mV	–10		+10	
$V_{\text{BCN}}$	BAT_SN – VSS +Fault (BCN) Threshold Range <sup>(1)</sup>	Recommended threshold range. Factory trimmed in $\approx 2$ -mV steps	+100		+250	mV
	Factory default trimmed threshold <sup>(3)</sup>			+200		
$V_{\text{BCN\_ACC}}$	BAT_SN – VSS +Fault Accuracy <sup>(3)</sup>	RLO mode enabled, Step size 10 mV	–10		+10	

### 6.5.4 Cell Sensing Output (BAT\_SP, BAT\_SN) (continued)

Unless otherwise noted, characteristics noted under conditions of  $T_A = -40$  to  $85^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{BDN}$	BAT_SN – VSS –Fault (BDN) Threshold Range <sup>(1)</sup>	Recommended threshold range. Factory trimmed in $\approx 2$ -mV steps	-250	-200	-100	mV
	Factory default trimmed threshold <sup>(3)</sup>					
$V_{BDN\_ACC}$	BAT_SN – VSS –Fault Accuracy <sup>(3)</sup>	RLO mode enabled, Step size 10 mV	-10		+10	
$t_{LO\_FAULT\_DLY}$	BAT_SP / BAT_SN fault comparator delay <sup>(1)</sup>	8-ms delay		8		ms
		100-ms delay		100		ms
$t_{LO\_FAULT\_STRT}$	BAT_SP / BAT_SN fault restart time <sup>(1)</sup> <sup>(2)</sup>			1000		ms
<b>Transient Response</b>						
$V_{LOAD\_SP}$	BAT_SP load transient <sup>(1)</sup>	No load $\geq 1\text{ k}\Omega \geq$ No load, Transition time 1 $\mu\text{s}$	-300		300	mV
$V_{LOAD\_SN}$	BAT_SN load transient <sup>(1)</sup>		-200		200	mV
$V_{LINE\_SN}$	BAT_SN line transient <sup>(1)</sup>	$V_{BAT} = 1.5\text{ V} \geq 2.4\text{ V} \geq 1.5\text{ V}$ , Transition slope 500 mV / 10 $\mu\text{s}$	-30		30	mV
$V_{TRANS}$	(BAT_SP – BAT_SN) transition transient <sup>(1)</sup>	Firmware commanded transition from BUF mode to RLO mode	-700		50	mV

(1) Specified by Design. Not production tested.

(2) Firmware-based parameter. Not production tested.

(3) Accuracy assured by factory trim at specified default threshold. A change from the default threshold requires device calibration in the field. Refer to the [BQ27Z746 Technical Reference Manual](#).

### 6.5.5 Gauge Measurements (ADC, CC, Temperature)

Unless otherwise noted, characteristics noted under conditions of  $T_A = -40$  to  $85^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Analog Digital Converter (ADC)</b>						
$V_{BAT\_RES}$	Battery Voltage ADC Resolution (bits)	Signed data format, $\pm 15$ bits		16		bits
$V_{BAT\_FS}$	Battery Measurement Full Scale Range		-0.2		5.5	V
$V_{BAT\_ERR}$	Battery Voltage ADC Error	$T_A = +25^\circ\text{C}$ , $V_{BAT} = 4.0\text{ VDC}$		$\pm 1$		mV
		$V_{BAT} = 2.5$ to $5.0\text{ VDC}$		$\pm 2$		
$R_{BAT}$	Effective input resistance		8			$\text{M}\Omega$
$t_{BAT}$	Battery Voltage Conversion Time			11.7		ms
$V_{ADC\_RES}$	Effective Resolution	$V_{BAT}$	14	15		bits
<b>Coulomb Counter (CC)</b>						
$V_{CC\_CM}$	Common mode voltage range	$V_{SS} = 0\text{V}$ , $2\text{V} \leq V_{BAT} \leq 5\text{V}$	$V_{SS}$		$V_{BAT}$	V
$V_{CC\_IN}$	Input voltage range		$V_{CC\_CM} - 0.1$		$V_{CC\_CM} + 0.1$	V
$I_{CC\_IN}$	Effective input current sense range <sup>(1)</sup> <sup>(2)</sup>	Ideal $R_{SNS} = 1\text{ m}\Omega$ (16-bit data limited)		$\pm 32,768$		mA
		Ideal $R_{SNS} = 2\text{ m}\Omega$ (16-bit data limited)				
		Ideal $R_{SNS} = 5\text{ m}\Omega$		$\pm 20,000$		
$t_{CC\_CONV}$	Conversion time	Single conversion		1000		ms
$CC_{ADC\_RES}$	Effective Resolution			16		bits
		1 LSB = $V_{REF}1/10/(\pm 2^{15})$		$\pm 3.7$		$\mu\text{V}$

### 6.5.5 Gauge Measurements (ADC, CC, Temperature) (continued)

Unless otherwise noted, characteristics noted under conditions of  $T_A = -40$  to  $85^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC\_ERR}$	Effective current measurement error	Ideal $R_{SNS} = 1.0\text{ m}\Omega$ , $10.0\text{ A}$ , $T_A = 25^\circ\text{C}$		26		mA
		Ideal $R_{SNS} = 1.0\text{ m}\Omega$ , $-10.0\text{ A}$ , $T_A = 25^\circ\text{C}$		29		
$CC_{OSE}$	Offset error	16-bit Post-Calibration	-2.6	1.3	+2.6	LSB
$CC_{OSE\_DRIFT}$	Offset error drift	15-bit + sign, Post Calibration		0.04	0.07	LSB/ $^\circ\text{C}$
$CC_{GE}$	Gain Error	15-bit + sign, Over input voltage range	-492	131	+492	LSB
$R_{CC\_IN}$	Effective input resistance		7			M $\Omega$
<b>NTC Thermistor Measurement</b>						
$R_{NTC(PU)}$	Internal Pullup Resistance	Factory Trimmed, Firmware compensated	14.4	18	21.6	k $\Omega$
$R_{NTC(DRIFT)}$	Resistance drift over temperature	Firmware compensated	-250	-120	0	PPM/ $^\circ\text{C}$
$R_{NTC\_ERR}$	External NTC Thermistor Temperature Measurement Error with Linearization	Ideal 10K $\Omega$ 103AT NTC, $T_A = -10$ to $70^\circ\text{C}$	-2	$\pm 1$	+2	$^\circ\text{C}$
		Ideal 10K $\Omega$ 103AT NTC, $T_A = -40$ to $85^\circ\text{C}$	-3	$\pm 2$	+3	
<b>Internal Temperature Sensor</b>						
$V_{(TEMP)}$	Internal Temperature sensor voltage drift	$V_{TEMPP}$	1.65	1.73	1.8	mV/ $^\circ\text{C}$
$V_{(TEMP)}$	Internal Temperature sensor voltage drift	$V_{TEMPP} - V_{TEMPN}$ (specified by design)	0.17	0.18	0.19	mV/ $^\circ\text{C}$

- (1) Firmware-based parameter. Not production tested.
- (2) Limited by 16-bit twos-complement numeric format

### 6.5.6 Flash Memory

Unless otherwise noted, characteristics noted under conditions of  $T_A = -40$  to  $85^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Data retention		10	100		Years
	Flash programming write cycles	Data Flash	20000			Cycles
		Instruction Flash	1000			Cycles
$t_{(ROWPROG)}$	Row programming time				40	$\mu\text{s}$
$t_{(MASSERASE)}$	Mass-erase time	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$			40	ms
$t_{(PAGEERASE)}$	Page-erase time	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$			40	ms
$I_{FLASHREAD}$	Flash Read Current	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$			1	mA
$I_{FLASHWRITE}$	Flash Write Current	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$			5	mA
$I_{FLASHERASE}$	Flash Erase Current	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$			15	mA

### 6.6 Digital I/O: DC Characteristics

Unless otherwise noted, characteristics noted under conditions of  $T_A = -40$  to  $85^\circ\text{C}$ ,  $V_{REG18} = 1.8\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>I<sup>2</sup>C Pins (SCL, SDA/HDQ)</b>						
$V_{IH}$	High-level input voltage	SCL, SDA pins	1.26			V
$V_{IL}$	Low-level input voltage low	SCL, SDA pins			0.54	V
$V_{OL}$	Low-level output voltage	SCL, SDA pins, $I_{OL} = 1\text{ mA}$			0.36	V
$C_i$	Input capacitance	SCL, SDA pins			10	pF

## 6.6 Digital I/O: DC Characteristics (continued)

Unless otherwise noted, characteristics noted under conditions of  $T_A = -40$  to  $85^\circ\text{C}$ ,  $V_{\text{REG18}} = 1.8\text{ V}$

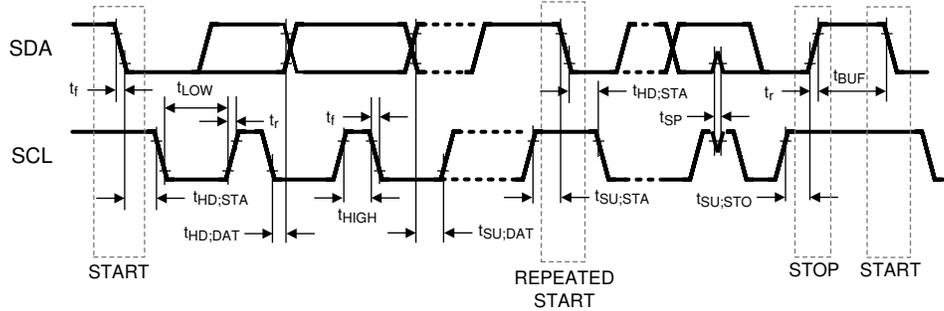
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{\text{Ikg}}$	Input leakage current	SCL, SDA pins		1		$\mu\text{A}$
<b>Push-Pull Pins (GPO)</b>						
$V_{\text{IH}}$	High-level input voltage	Push-Pull pins	1.15			V
$V_{\text{IL}}$	Low-level input voltage low	Push-Pull pins			0.54	V
$V_{\text{OH}}$	Output voltage high	Push-Pull pins, $I_{\text{OH}} = -1\text{ mA}$	1.08			V
$V_{\text{OL}}$	Output voltage low	Push-Pull pins, $I_{\text{OL}} = 1\text{ mA}$			0.36	V
$C_{\text{I}}$	Input capacitance	Push-Pull pins			10	pF
$I_{\text{Ikg}}$	Input leakage current	Push-Pull pins		1		$\mu\text{A}$

## 6.7 Digital I/O: Timing Characteristics

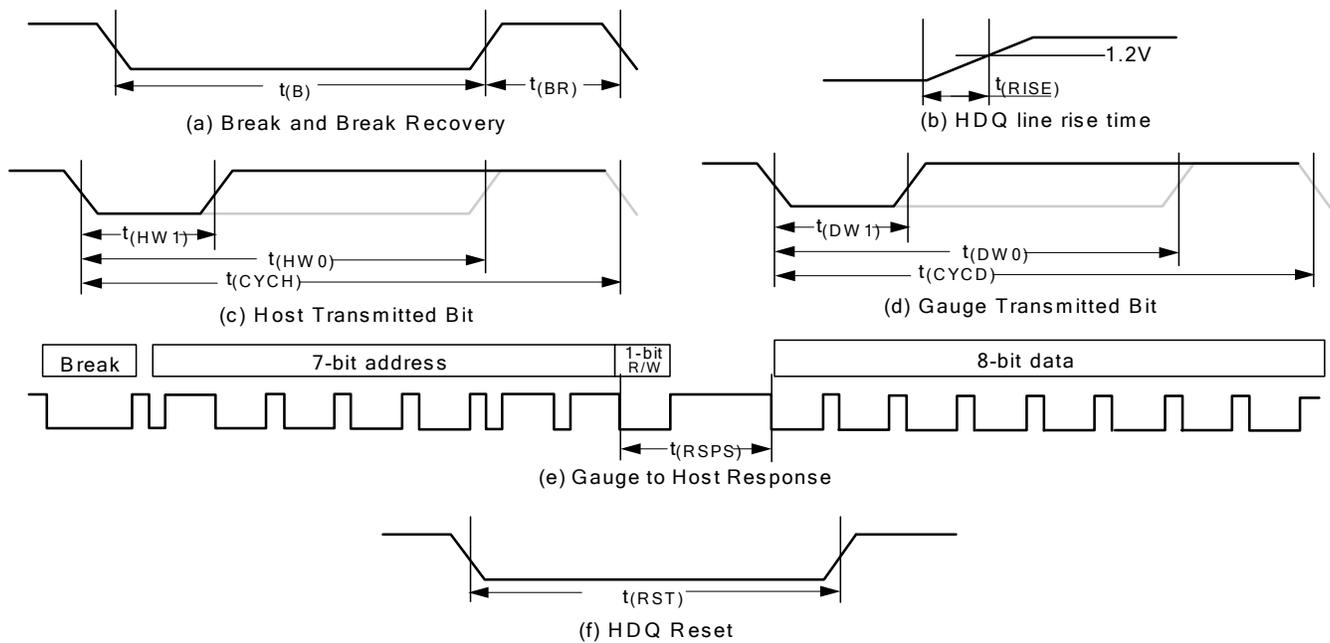
PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
<b>I<sup>2</sup>C Timing — 100 kHz</b>						
$f_{\text{SCL}}$	Clock Operating Frequency	SCL duty cycle = 50%			100	kHz
$t_{\text{HD:STA}}$	START Condition Hold Time		4.0			$\mu\text{s}$
$t_{\text{LOW}}$	Low period of the SCL Clock		4.7			$\mu\text{s}$
$t_{\text{HIGH}}$	High period of the SCL Clock		4.0			$\mu\text{s}$
$t_{\text{SU:STA}}$	Setup repeated START		4.7			$\mu\text{s}$
$t_{\text{HD:DAT}}$	Data hold time (SDA input)		0			ns
$t_{\text{SU:DAT}}$	Data setup time (SDA input)		250			ns
$t_{\text{r}}$	Clock Rise Time	10% to 90%			1000	ns
$t_{\text{f}}$	Clock Fall Time	90% to 10%			300	ns
$t_{\text{SU:STO}}$	Setup time STOP Condition		4.0			$\mu\text{s}$
$t_{\text{BUF}}$	Bus free time STOP to START		4.7			$\mu\text{s}$
<b>I<sup>2</sup>C Timing — 400 kHz</b>						
$f_{\text{SCL}}$	Clock Operating Frequency	SCL duty cycle = 50%			400	kHz
$t_{\text{HD:STA}}$	START Condition Hold Time		0.6			$\mu\text{s}$
$t_{\text{LOW}}$	Low period of the SCL Clock		1.3			$\mu\text{s}$
$t_{\text{HIGH}}$	High period of the SCL Clock		600			ns
$t_{\text{SU:STA}}$	Setup repeated START		600			ns
$t_{\text{HD:DAT}}$	Data hold time (SDA input)		0			ns
$t_{\text{SU:DAT}}$	Data setup time (SDA input)		100			ns
$t_{\text{r}}$	Clock Rise Time	10% to 90%			300	ns
$t_{\text{f}}$	Clock Fall Time	90% to 10%			300	ns
$t_{\text{SU:STO}}$	Setup time STOP Condition		0.6			$\mu\text{s}$
$t_{\text{BUF}}$	Bus free time STOP to START		1.3			$\mu\text{s}$
<b>HDQ Timing</b>						
$t_{\text{B}}$	Break Time		190			$\mu\text{s}$
$t_{\text{BR}}$	Break Recovery Time		40			$\mu\text{s}$
$t_{\text{HW1}}$	Host Write 1 Time	Host drives HDQ	0.5		50	$\mu\text{s}$
$t_{\text{HW0}}$	Host Write 0 Time	Host drives HDQ	86		145	$\mu\text{s}$
$t_{\text{CYCH}}$	Cycle Time, Host to device	device drives HDQ	190			$\mu\text{s}$
$t_{\text{CYCD}}$	Cycle Time, device to Host	device drives HDQ	190	205	250	$\mu\text{s}$
$t_{\text{DW1}}$	Device Write 1 Time	device drives HDQ	32		50	$\mu\text{s}$

### 6.7 Digital I/O: Timing Characteristics (continued)

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{DW0}$	Device Write 0 Time	device drives HDQ		145	$\mu\text{s}$
$t_{RSPS}$	Device Response Time	device drives HDQ		950	$\mu\text{s}$
$t_{TRND}$	Host Turn Around Time	Host drives HDQ after device drives HDQ			$\mu\text{s}$
$t_{RISE}$	HDQ Line Rising Time to Logic 1			1.8	$\mu\text{s}$
$t_{RST}$	HDQ Reset	Host drives HDQ low before device reset		2.2	s



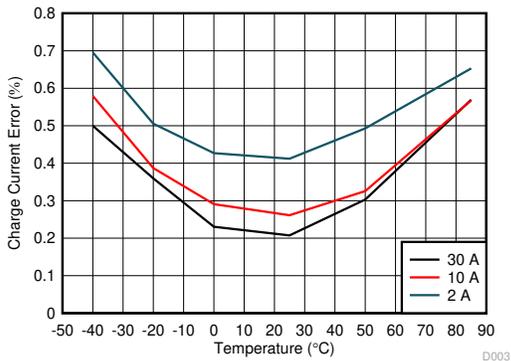
6-1. I<sup>2</sup>C Timing



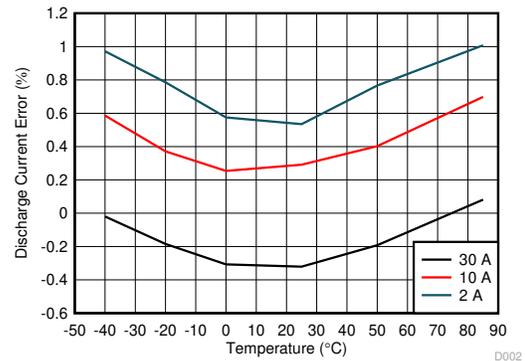
- a. HDQ Breaking
- b. Rise time of HDQ line
- c. HDQ Host to fuel gauge communication
- d. Fuel gauge to Host communication
- e. Fuel gauge to Host response format
- f. HDQ Host to fuel gauge

6-2. HDQ Timing

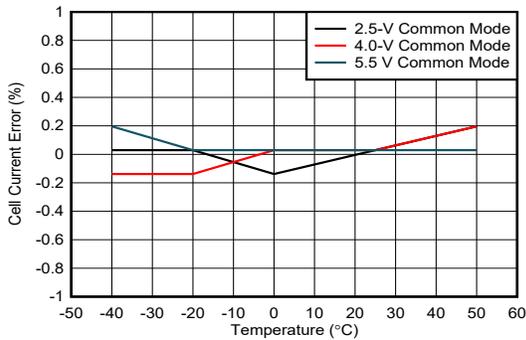
## 6.8 Typical Characteristics



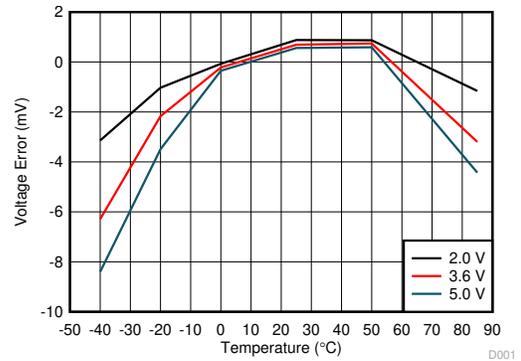
**6-3. Charge Current Error vs Temperature and Charger Current with 1-mΩ sense, No Calibration**



**6-4. Discharge Current Error vs Temperature and Load Current with 1mΩ Sense, No Calibration**



**6-5. 2.2A Current Error vs CC ADC Input Common Mode Voltage and Temperature, No Calibration**



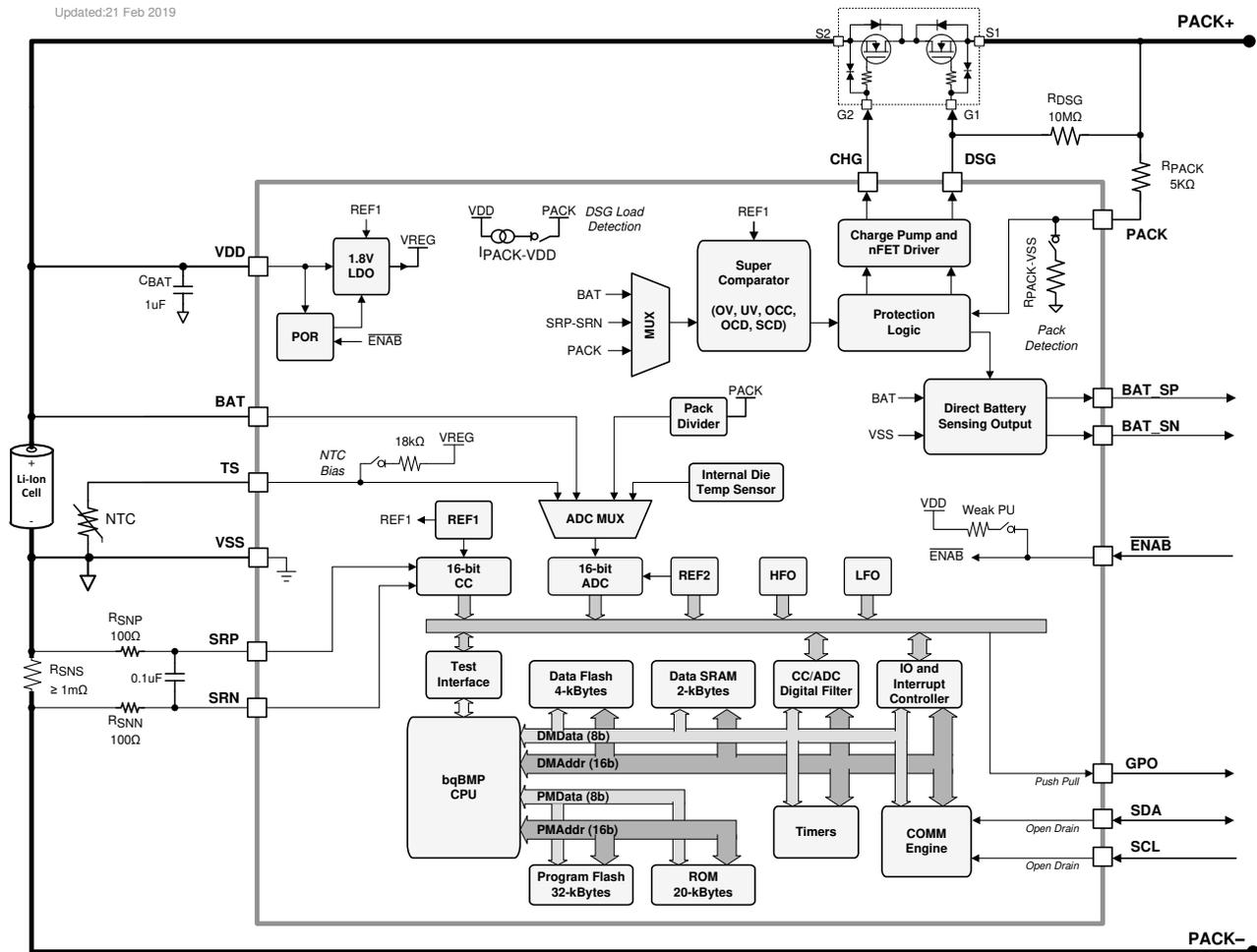
**6-6. Cell Voltage Error vs Battery Voltage and Temperature**

## 7 Detailed Description

### 7.1 Overview

The BQ27Z746 gas gauge is a fully integrated battery manager that employs flash-based firmware to provide a complete solution for battery-stack architectures composed of 1-series cells. The BQ27Z746 device interfaces with a host system through an I<sup>2</sup>C or HDQ protocol. High-performance, integrated analog peripherals enable support for a sense resistor down to 1 mΩ, and simultaneous current/voltage data conversion for instant power calculations. The following sections detail all of the major component blocks included as part of the BQ27Z746 device.

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 BQ27Z746 Processor

The BQ27Z746 device uses a custom TI-proprietary processor design that features a Harvard architecture and operates at frequencies up to 4.2 MHz. Using an adaptive, three-stage instruction pipeline, the BQ27Z746 processor supports variable instruction lengths of 8, 16, or 24 bits.

### 7.3.2 Battery Parameter Measurements

The BQ27Z746 device measures cell voltage and current simultaneously, and also measures temperature to calculate the information related to remaining capacity, full charge capacity, state-of-health, and other gauging parameters.

#### 7.3.2.1 Coulomb Counter (CC) and Digital Filter

The first ADC is an integrating analog-to-digital converter designed specifically for tracking charge and discharge activity, or coulomb counting, of a rechargeable battery. It features a single-channel differential input that converts the voltage difference across a sense resistor between the SRP and SRN terminals with a resolution of 3.74  $\mu\text{V}$ . The differential input common mode voltage range is from  $V_{SS}$  to  $V_{BAT}$  and supports a 1-series cell high-side or low-side sensing option with  $\pm 0.1\text{-V}$  input range. The CC digital filter generates a 16-bit conversion value from the delta-sigma CC front-end. New conversions are available every 1 s.

#### 7.3.2.2 ADC Multiplexer

The ADC multiplexer provides selectable connections to the external pins, BAT and TS, as well as the internal temperature sensor. In addition, the multiplexer can independently enable the TS input connection to the internal thermistor biasing circuitry, and enables the user to short the multiplexer inputs for test and calibration purposes.

#### 7.3.2.3 Analog-to-Digital Converter (ADC)

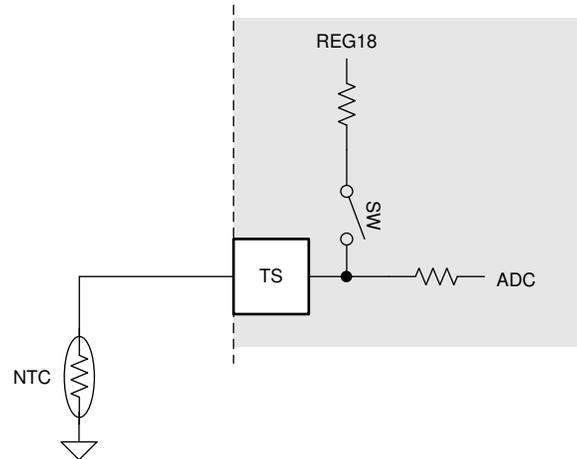
The second ADC is a 16-bit delta-sigma converter designed for general-purpose measurements. The ADC automatically scales the input voltage range during sampling based on channel selection. The converter resolution is a function of its full-scale range and number of bits, yielding a 38- $\mu\text{V}$  resolution.

#### 7.3.2.4 Internal Temperature Sensor

An internal temperature sensor is available on the BQ27Z746 device to reduce the cost, power, and size of the external components necessary to measure temperature. It is available for connection to the ADC using the multiplexer, and is ideal for quickly determining pack temperature under a variety of operating conditions.

#### 7.3.2.5 External Temperature Sensor Support

The TS input is enabled with an internal 18-k $\Omega$  (Typ.) linearization pull-up resistor to support the use of a 10-k $\Omega$  (25°C) NTC external thermistor, such as the Semitec 103AT-2. The NTC thermistor should be connected between  $V_{SS}$  and the individual TS pin. The analog measurement is then taken by the ADC through its input multiplexer. If a different thermistor type is required, then changes to configurations may be required.



**7-1. External Thermistor Biasing**

### 7.3.3 Power Supply Control

The BQ27Z746 device uses the VDD pin as its power source. VDD powers the internal voltage sources that supply references for the device. The BAT pin is a non-current carrying path and used as a Kelvin sense connection to the battery cell.

### 7.3.4 Bus Communication Interface

The BQ27Z746 device has an I<sup>2</sup>C bus communication interface. Alternatively, the device can be configured to communicate through the HDQ pin (shared with SDA).

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#### Note

Once the device is switched to the HDQ protocol, it is not reversible.

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### 7.3.5 Low Frequency Oscillator

The BQ27Z746 device includes a low frequency oscillator (LFO) running at 65.536 kHz.

### 7.3.6 High Frequency Oscillator

The BQ27Z746 includes a high frequency oscillator (HFO) running at 16.78 MHz. It is frequency locked to the LFO output and scaled down to 8.388 MHz with a 50% duty cycle.

### 7.3.7 1.8-V Low Dropout Regulator

The BQ27Z746 device contains an integrated capacitor-less 1.8-V LDO (REG18) that provides regulated supply voltage for the device CPU and internal digital logic.

### 7.3.8 Internal Voltage References

The BQ27Z746 device provides two internal voltage references. REF1 is used by REG18, oscillators, and CC. REF2 is used by the ADC.

### 7.3.9 Overcurrent in Discharge Protection

The overcurrent in discharge (OCD) function detects abnormally high current in the discharge direction. The overload in discharge threshold and delay time are configurable through the firmware register. The thresholds and timing can be fine-tuned even further based on a sense resistor with lower resistance or wider tolerance through calibration. When an OCD event occurs, the **Safety Status** flag is set to 1 and is latched until it is cleared and the fault condition is removed.

### 7.3.10 Overcurrent in Charge Protection

The short-circuit current in charge (OCC) function detects catastrophic current conditions in the charge direction. The short-circuit in charge threshold and delay time are configurable through the firmware register. The thresholds and timing can be fine-tuned even further based on a sense resistor with lower resistance or wider tolerance through calibration. The detection circuit also incorporates a blanking delay before disabling the CHG and DSG FETs. When an OCC event occurs, the **Safety Status** flag bit is set to 1 and is latched until it is cleared and the fault condition is removed.

### 7.3.11 Short-Circuit Current in Discharge Protection

The short-circuit current in discharge (SCD) function detects catastrophic current conditions in the discharge direction. The short-circuit in discharge thresholds and delay times are configurable through the firmware register. The thresholds and timing can be fine-tuned even further based on a sense resistor with lower resistance or wider tolerance with calibration. The detection circuit also incorporates a delay before disabling the CHG and DSG FETs. When an SCD event occurs, the **Safety Status** flag bit is set to 1 and is latched until it is cleared and the fault condition is removed.

### 7.3.12 Primary Protection Features

The BQ27Z746 gas gauge supports the following battery and system level protection features, which can be configured using firmware:

- Cell Undervoltage Protection
- Cell Overvoltage Protection
- Overcurrent in CHARGE Mode
- Overcurrent in DISCHARGE Mode
- Overload in DISCHARGE Mode
- Short Circuit in DISCHARGE Mode
- Overtemperature in CHARGE Mode
- Overtemperature in DISCHARGE Mode
- Precharge Timeout
- Fast Charge Timeout

### 7.3.13 Battery Sensing

The BQ27Z746 offers direct battery sensing through differential battery sensing pins BAT\_SP and BAT\_SN for accurate battery voltage measurement and detection. BQ27Z746 battery sensing path includes protection and isolation to minimize any leakage and coupling issue. The cell isolation includes a combination of buffered and resistive options. Firmware configuration allows seamless auto-transition between the two sensing schemes. The battery sensing buffer is powered from the PACK pin.

For accurate battery voltage sensing when using the sensing buffer, the PACK pin must be powered and  $V_{PACK} > V_{BAT} + 0.7$  V. The sensing protection thresholds (BCP, BCN, BDP, and BDN) provide short detection for the battery sensing output pins, and places the battery sensing output pins in a high impedance state when triggered. The BQ27Z746 battery sensing has firmware programmable offset options for applications where differential output voltage needs to be shifted to overcome an input range limitation. The offset voltage selected should never exceed the sensing protection thresholds, because this causes false battery sensing faults.

### 7.3.14 Gas Gauging

This device uses the Impedance Track™ technology to measure and determine the available charge in battery cells. See the [Theory and Implementation of Impedance Track Battery Fuel-Gauging Algorithm Application Report](#) for further details.

### 7.3.15 Zero Volt Charging (ZVCHG)

ZVCHG (0-V charging) is a special function that allows charging a severely depleted battery that is below the FET driver charge pump shutdown voltage ( $V_{FET\_SHUT}$ ). The BQ27Z746 has ZVCHG enabled. If  $V_{BAT} > V_{OINH}$  and  $V_{BAT} < V_{FET\_SHUT}$  and the charger voltage at PACK+ is  $> V_{OCHGR}$ , then the CHG output will be driven to the voltage of the PACK pin, allowing charging. ZVCHG mode in the BQ27Z746 is exited when  $V_{BAT} >$

$V_{FET\_SHUT\_REL}$ , at which point the charge pump is enabled, and CHG transitions to being driven by the charge pump. For BQ27Z746, when the voltage on VDD is below  $V_{0INH}$ , the CHG output becomes high impedance, and any leakage current flowing through the CHG FET may cause this voltage to rise and reenabling charging. If this is undesired, a high impedance resistor can be included between the CHG FET gate and source to overcome any leakage and ensure the FET remains disabled in this case. This resistance should be as high as possible while still ensuring the FET is disabled, since it will increase the device operating current when the CHG driver is enabled. Because gate leakage is typically extremely low, a gate-source resistance of 50 M $\Omega$  to 100 M $\Omega$  may be sufficient to overcome the leakage.

### 7.3.16 Charge Control Features

This device supports charge control features, such as:

- Reports charging voltage and charging current based on the active temperature range—JEITA temperature ranges T1, T2, T3, T4, T5, and T6
- Provides more complex charging profiles, including sub-ranges within a standard temperature range
- Reports the appropriate charging current required for constant current charging, and the appropriate charging voltage needed for constant voltage charging to a smart charger, using the bus communication interface
- Selects the chemical state-of-charge of each battery cell using the Impedance Track method
- Provides pre-charging/zero-volt charging
- Employs charge inhibit and charge suspend if battery pack temperature is out of programmed range
- Activates charge and discharge alarms to report charging faults and to indicate charge status

### 7.3.17 Authentication

This device supports security with the following features, which can be enabled if desired:

- Authentication by the host using the SHA-256 method
- The gas gauge requires SHA-256 authentication before the device can be unsealed or allow full access.

## 7.4 Device Functional Modes

This device supports five modes, but the current consumption varies, based on firmware control of certain functions and modes of operation:

- **NORMAL mode:** In this mode, the device performs measurements, calculations, protections, and data updates every 250-ms intervals. Between these intervals, the device operates in a reduced power state to minimize total average current consumption. Battery protections are continuously monitored and both protection NFETs are typically on.
- **SLEEP mode:** In this mode, the device performs measurements, calculations, and data updates in adjustable time intervals. Between these intervals, the device operates in a reduced power stage to minimize total average current consumption. Battery protections are continuously monitored and both protection NFETs are typically on.
- **SHIP mode:** In this mode, the device measures voltage and temperature very infrequently and at shorter ADC conversion times, and current is not measured or coulomb counted. Current is assumed to be, and reported as, 0 mA. Therefore, the device tracks the battery's state-of-charge from OCVs. The measurements performed each interval are cell voltage, temperature, and PACK voltage (every fourth interval). Processing is minimized by reducing the number of calculations. Some calculations are performed less frequently: only after voltage and temperature are measured. These less frequent calculations include updating firmware-based protections, lifetime data, and the voltage and temperature ranges of the advanced charge algorithm. Other calculations, such as updating *RemainingCapacity()* and *FullChargeCapacity()*, are not performed at all with the assumption the system is off and will not communicate with the gauge. Battery protections are continuously monitored and both protection NFETs remain on, typically.
- **SHELF mode:** In this mode, power consumption is reduced even further from SHIP mode by turning off the CHG and DSG NFETs and all hardware-based protections. Due to this, no external power is available to the system in SHELF mode. The device measures voltage and temperature very infrequently and at shorter ADC conversion times, and current is not measured or coulomb counted. Current is assumed to be, and reported as, 0 mA. Therefore, the device tracks the battery's state-of-charge from voltage measurements. The measurements performed each interval are cell voltage, temperature and PACK voltage (every fourth interval). Processing is minimized by reducing the number of calculations. Some calculations are performed

less frequently: only after voltage and temperature are measured. These less frequent calculations include updating firmware-based protections, lifetime data, and the voltage and temperature ranges of the advanced charge algorithm. Other calculations, such as updating *RemainingCapacity()* and *FullChargeCapacity()*, are not performed at all with the assumption the system is off and will not communicate with the gauge.

- SHUTDOWN mode: In this mode, the device is completely disabled to minimize power consumption and to avoid depleting the battery.

#### 7.4.1 Lifetime Logging Features

The device supports data logging of several key parameters for warranty and analysis:

- Maximum and minimum cell temperature
- Maximum current in CHARGE or DISCHARGE mode
- Maximum and minimum cell voltages
- Safety events and number of occurrences

#### 7.4.2 Configuration

The device supports accurate data measurements and data logging of several key parameters.

##### 7.4.2.1 Coulomb Counting

The device uses an integrating delta-sigma analog-to-digital converter (ADC) for current measurement. The ADC measures charge/discharge flow of the battery by measuring the voltage across a very small external sense resistor. The integrating ADC measures a bipolar signal from a range of  $-100\text{ mV}$  to  $100\text{ mV}$ , with a positive value when  $V_{(SRP)} - V_{(SRN)}$ , indicating charge current and a negative value indicating discharge current.

The current measurement is performed by measuring the voltage drop across the external sense resistor, which can be as low as  $1\text{ m}\Omega$ , and the polarity of the differential voltage determines if the cell is in the CHARGE or DISCHARGE mode.

##### 7.4.2.2 Cell Voltage Measurements

The BQ27Z746 gas gauge measures the cell voltage at 1-s intervals using the ADC. This measured value is internally scaled for the ADC and is calibrated to reduce any errors due to offsets. This data is also used for calculating the impedance of the cell for Impedance Track gas gauging.

##### 7.4.2.3 Auto Calibration

The auto-calibration feature helps to cancel any voltage offset across the SRP and SRN pins for accurate measurement of the cell voltage, charge/discharge current, and thermistor temperature. The auto-calibration is performed when there is no communication activity for a minimum of 5 s on the bus lines.

##### 7.4.2.4 Temperature Measurements

This device has an internal sensor for on-die temperature measurements, and the ability to support an external temperature measurement through the external NTC on the TS pin. These two measurements are individually enabled and configured.

## 8 Applications and Implementation

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

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### 8.1 Application Information

The BQ27Z476 can be used with a 1-series Li-ion/Li polymer battery pack. To implement and design a comprehensive set of parameters for a specific battery pack, the user needs Battery Management Studio (BQStudio), which is a graphical user-interface tool installed on a PC during development. The firmware installed

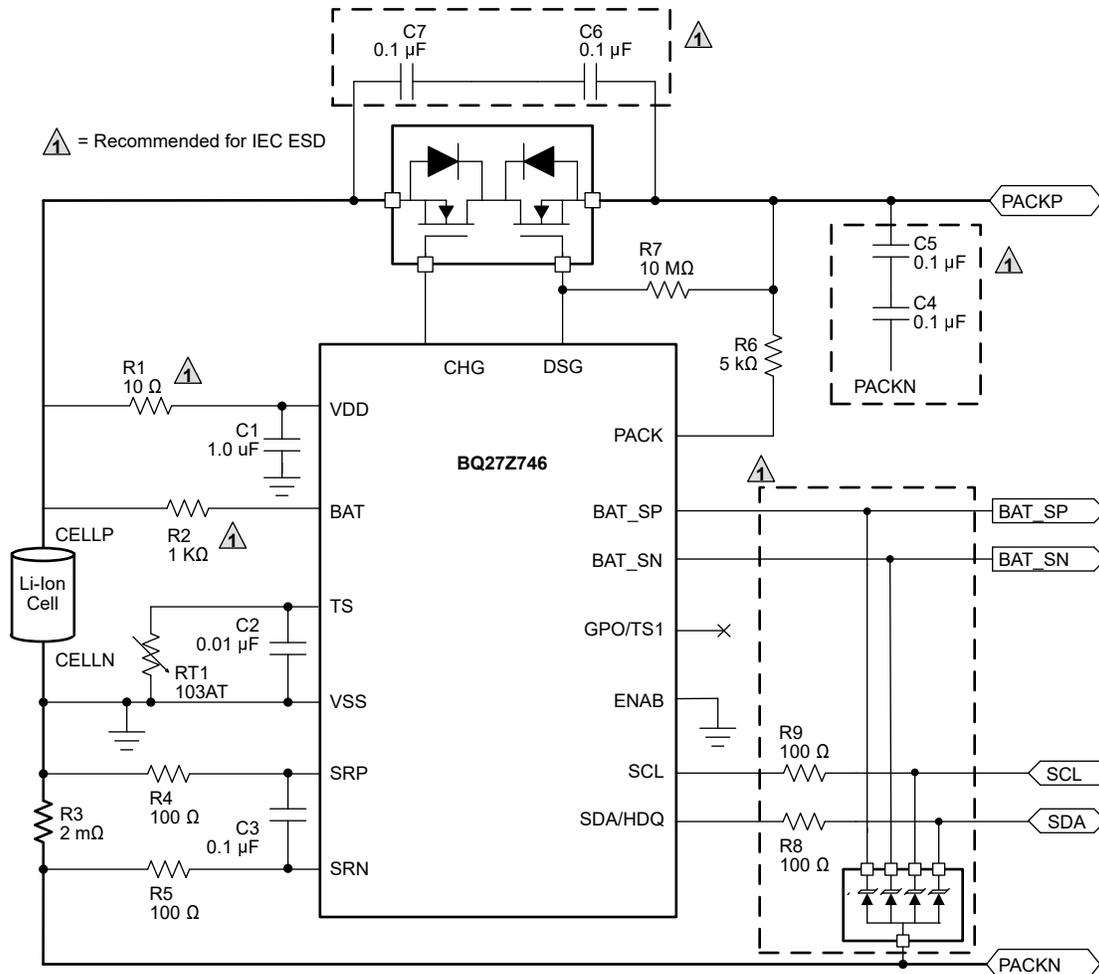
**BQ27Z746**

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in the product has default values, which are summarized in the associated [BQ27Z476 Technical Reference Manual \(SLUUCA6\)](#). Using the BQStudio tool, these default values can be changed to cater to specific application requirements during development once the system parameters, such as enable or disable certain features for operation, cell configuration, chemistry that best matches the cell used, and more. The final flash image, which is extracted once configuration and testing are complete, is used for mass production and is referred to as the "golden image."

**8.2 Typical Applications**

The following is an example BQ27Z476 application schematic for a single-cell battery pack.



**8-1. BQ27Z746 1-Series Cell Low Side Current Sensing Typical Implementation**

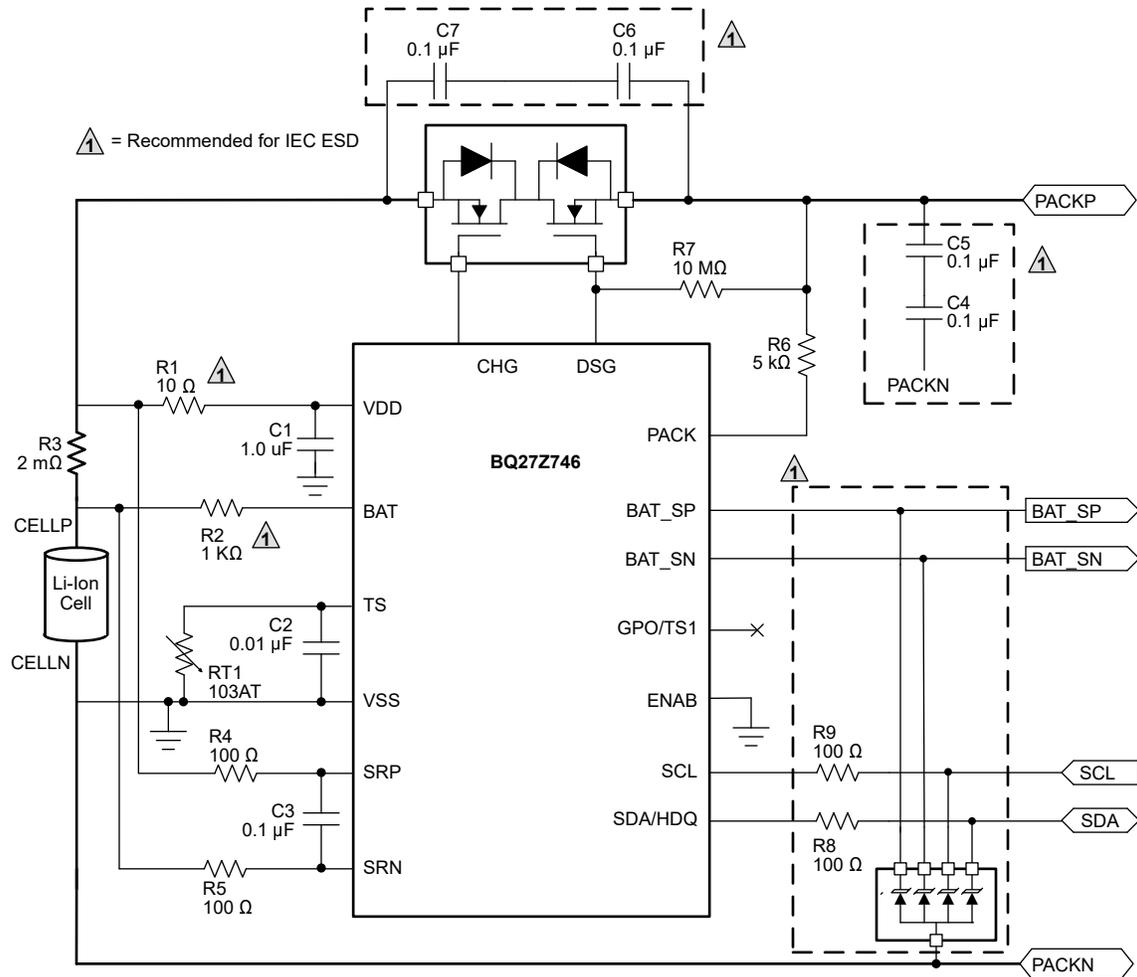


图 8-2. BQ27Z746 1-Series Cell High Side Current Sensing Typical Implementation

### 8.2.1 Design Requirements (Default)

Design Parameter	Example
Cell Configuration	1s1p (1 series with 1 parallel)
Design Capacity	5300 mAh
Device Chemistry	Li-Ion
Design Voltage	4000 mV
Cell Low Voltage	2500 mV

### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 Changing Design Parameters

For the firmware settings needed for the design requirements, refer to the [BQ27Z746 Technical Reference Manual \(SLUUCA6\)](#).

- To change design capacity, set the data flash value (in mAh) in the **Gas Gauging: Design: Design Capacity** register.
- To set device chemistry, go to the data flash **I<sup>2</sup>C Configuration: Data: Device Chemistry**. The BQStudio software automatically populates the correct chemistry identification. This selection is derived from using the BQCHEM feature in the tools and choosing the option that matches the device chemistry from the list.
- To set the design voltage, go to **Gas Gauging: Design: Design Voltage** register.

- To set the cell **Low Voltage** or clear the cell **Low Voltage**, use **Settings: Configuration: Init Voltage Low Set** or **Clear**. This is used to set the cell voltage level that will set (clear) the [VOLT\_LO] bit in the *Interrupt Status* register.
- To enable the internal temperature and the external temperature sensors: Set **Settings: Configuration: Temperature Enable**: Bit 0 (TSInt) = 1 for the internal sensor; set Bit 1 (TS1) = 1 for the external sensor.

### 8.2.3 Calibration Process

The calibration of current, voltage, and temperature readings is accessible by writing 0xF081 or 0xF082 to *ManufacturerAccess()*. A detailed procedure is included in the [BQ27Z746 Technical Reference Manual \(SLUUCA6\)](#) in the *Calibration* section. The description allows for calibration of cell voltage measurement offset, battery voltage, current calibration, coulomb counter offset, PCB offset, CC gain/capacity gain, and temperature measurement for both internal and external sensors.

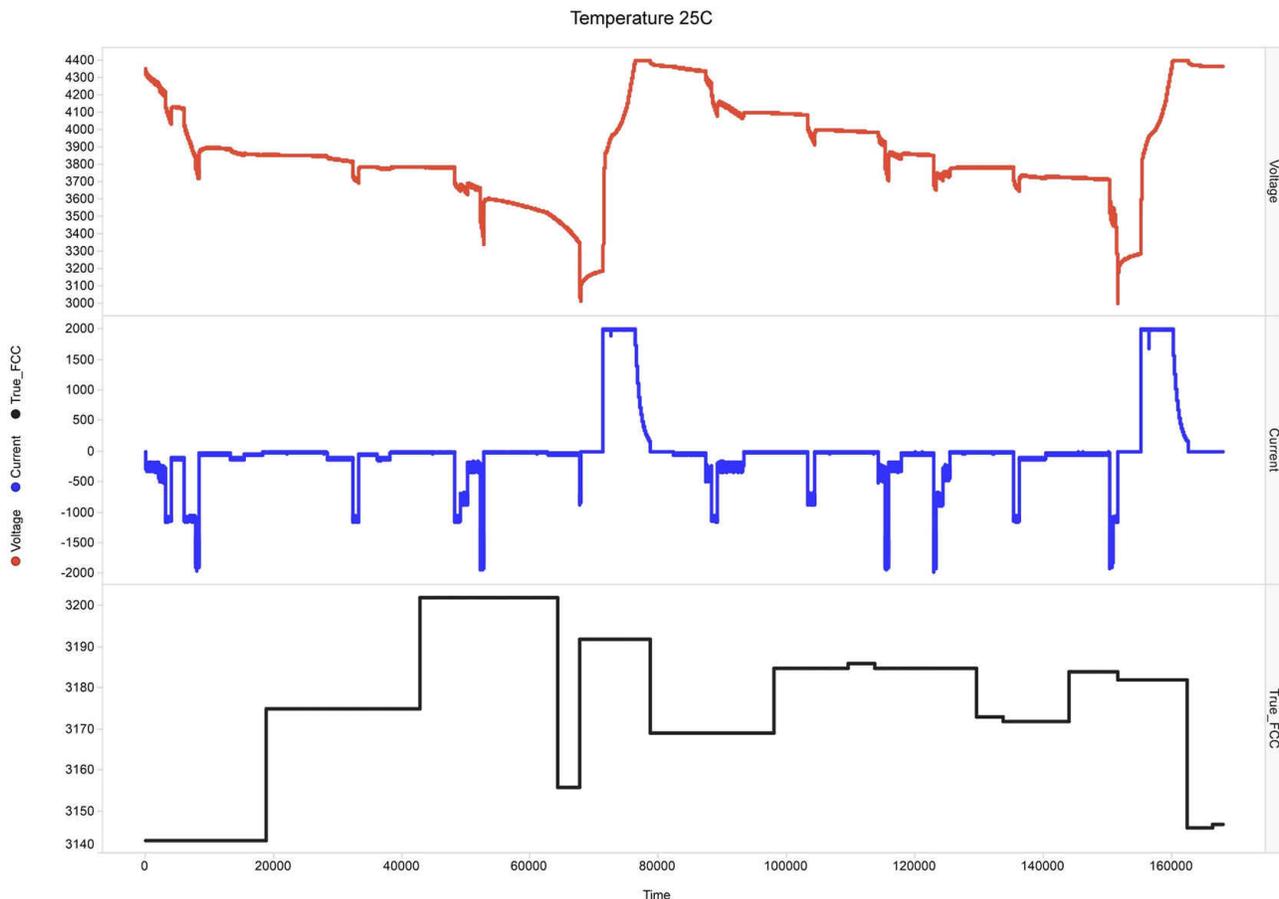
### 8.2.4 Gauging Data Updates

When a battery pack enabled with the BQ27Z746 gas gauge is cycled, the value of *FullChargeCapacity()* updates several times, including the onset of charge or discharge, charge termination, temperature delta, resistance updates during discharge, and relaxation. [Figure 8-3](#) shows actual battery voltage, load current, and *FullChargeCapacity()* when some of those updates occur during a single application cycle.

Update points from the plot include:

- Charge termination at 7900 s
- Relaxation at 9900 s
- Resistance update at 11500 s

#### 8.2.4.1 Application Curve



**Figure 8-3. Full Charge Capacity Tracking (X-Axis Is Seconds)**

## 9 Power Supply Requirements

The BQ27Z746 device uses the VDD pin as its power source. VDD pin powers the internal voltage sources that supply references for the device. The VDD pin connects to 1-series battery cells' positive terminal and supports a minimum of 2 V to a maximum of 5 V. The BAT pin is a noncurrent carrying path and is used as a battery voltage Kelvin sense connection to the 1-series battery cells' positive terminal.

## 10 Layout

### 10.1 Layout Guidelines

- The quality of the Kelvin connections at the sense resistor is critical. The sense resistor must have a temperature coefficient no greater than 50 ppm to minimize current measurement drift with temperature. Choose the value of the sense resistor to correspond to the available overcurrent and short-circuit ranges of the BQ27Z746 gas gauge. Select the smallest value possible to minimize thermal dissipation and still maintain required measurement accuracy. The value of the sense resistor impacts the differential voltage generated across the BQ27Z746 SRP and SRN nodes during a short circuit. These pins have a differential voltage should not exceed  $V_{CC\_IN}$  of  $\pm 0.1$  V for normal operation. Parallel sense resistors can be used as long as good Kelvin sensing is ensured. The device is designed to support a 1-m $\Omega$  to 20-m $\Omega$  sense resistor.
- BAT should be tied directly to the positive connection of the battery with a series 1-k $\Omega$  resistor. It should not share a path with the VDD pin and its 10- $\Omega$  series resistor.
- In reference to the gas gauge circuit, the following features require attention for component placement and layout: VDD bypass capacitor, SRN and SRP differential low-pass filter, and I<sup>2</sup>C communication ESD external protection.
- The BQ27Z746 gas gauge uses an integrating delta-sigma ADC for current measurements. Add a 100- $\Omega$  resistor from the sense resistor to the SRP and SRN inputs of the device. Place a 0.1- $\mu$ F filter capacitor across the SRP and SRN inputs. Place all filter components as close as possible to the device. Route the traces from the sense resistor as differential pairs to the filter circuit. Adding a ground plane around the filter network can provide additional noise immunity.
- The BQ27Z746 has an internal LDO that is internally compensated and does not require an external decoupling capacitor.
- The I<sup>2</sup>C clock and data pins have integrated high-voltage ESD protection circuits; however, adding a Zener diode and series resistor provides more robust ESD performance. The I<sup>2</sup>C clock and data lines have an internal pulldown. When the gas gauge senses that both lines are low (such as during removal of the pack), the device performs auto-offset calibration and then goes into SLEEP mode to conserve power.



## 11 Device and Documentation Support

### 11.1 Third-Party Products Disclaimer

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### 11.2 Documentation Support

#### 11.2.1 Related Documentation

- [BQ27Z746 Technical Reference Manual](#)
- [Theory and Implementation of Impedance Track Battery Fuel-Gauging Algorithm Application Report](#)

### 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.4 サポート・リソース

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### 11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Orderable, and Packaging Information

The following pages include mechanical, orderable, and packaging information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ27Z746YAHR	ACTIVE	DSBGA	YAH	15	3000	RoHS & Green	SAC396	Level-1-260C-UNLIM	-40 to 85	BQ27Z746	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

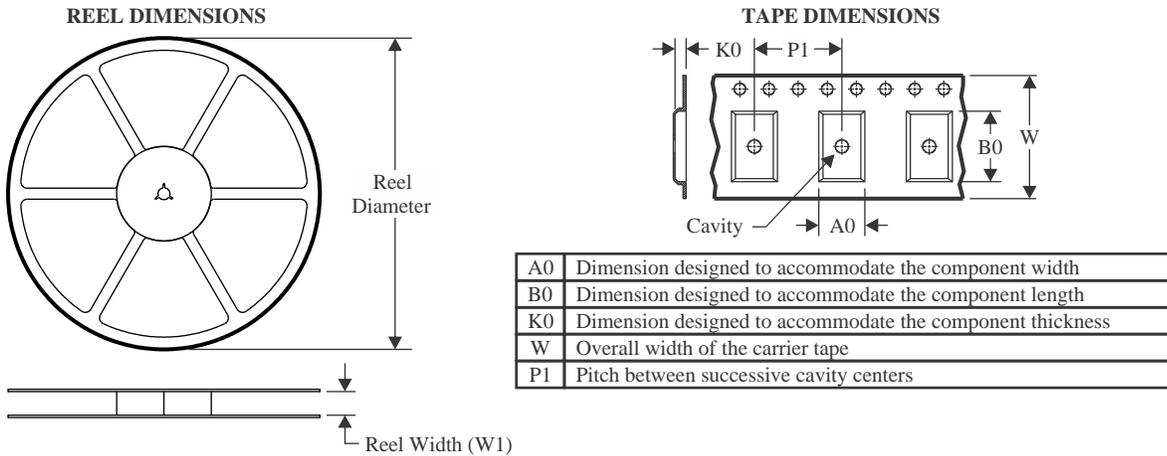
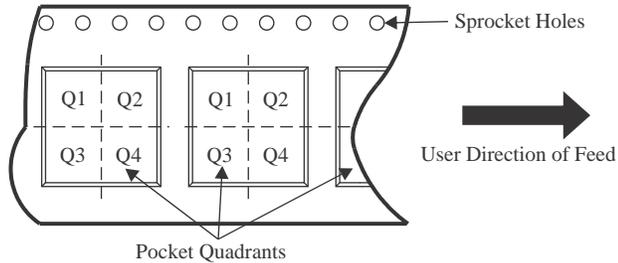
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

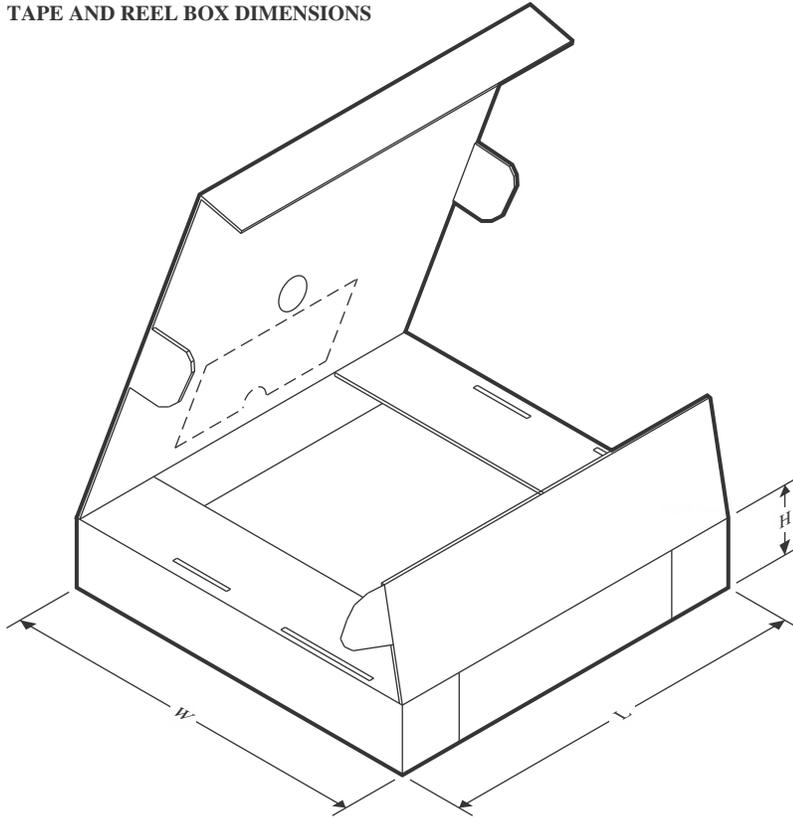
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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ27Z746YAHR	DSBGA	YAH	15	3000	180.0	12.4	1.88	2.76	0.55	4.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ27Z746YAHR	DSBGA	YAH	15	3000	182.0	182.0	20.0

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