TEXAS INSTRUMENTS
ADS9219, ADS9218, ADS9217
JAJSP59A – JANUARY 2023 – REVISED APRIL 2024

ADS921x デュアル、同時サンプリング、18 ビット、20MSPS、完全差動 ADC 入力ドライバ搭載、SAR 型 A/D コンバータ

1 特長

- 高速および低消費電力:
  - ADS9219:20MSPS/チャネル、172mW/チャネル
  - ADS9218:10MSPS/チャネル、140mW/チャネル
  - ADS9217:5MSPS/チャネル、90mW/チャネル
- 2 チャネル、同時サンプリング
- 内蔵機能:
  - ADC ドライバ
  - 高精度基準電圧
  - 同相電圧出力バッファ
- 高性能:
  - 18 ビット、ミッシング コードなし
  - INL:±1LSB、DNL:±0.75LSB
  - 信号対雑音比:OSR = 16 で 95.5dB および 104.5dB の SNR
- 広い入力帯域幅:
  - ADS9219:135MHz (-3dB)
  - ADS9218:90MHz (-3dB)
  - ADS9217:45MHz (-3dB)
- シリアル LVDS インターフェイス:
  - SDR および DDR 出力モード
  - 同期クロックおよびデータ出力
- 拡張動作範囲:-40℃～+125℃

2 アプリケーション

- 電力分析
- ソース メジャー ユニット (SMU)
- 海洋機器
- サーボ ドライブ位置フィードバック
- DC/AC 電源、電子負荷

3 概要

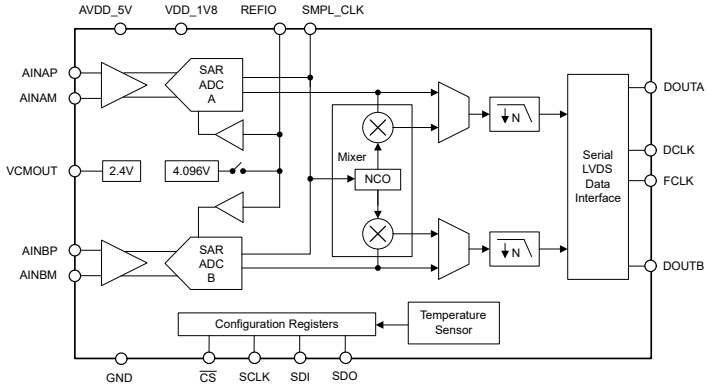
ADS921x は 18 ビット高速デュアルチャネル、同時サンプリングの A/D コンバータ (ADC) で、ADC 入力用のドライバが内蔵されています。ADC ドライバを内蔵しているため、信号チェーンの簡素化、高精度アプリケーションでの消費電力の低減、1MHz を上回る高周波信号のサポートが可能です。外付けデカップリング コンデンサを必要としない内蔵 ADC リファレンス バッファは、広帯域幅アプリケーション向けに最適化されています。

ADS921x は、シリアル LVDS (SLVDS) データ インターフェイスを使用して、デジタル スイッチング ノイズを最小化しながら高速デジタル通信を実現します。ADC チャネルごとに別々の SLVDS 出力、または両方の ADC チャネルに 1 つの SLVDS 出力を使用して、デュアル チャネル ADC データを読み取ります。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
ADS9218、ADS9219	RHA (VQFN、40)	6mm × 6mm
ADS9217 (3)	RHA (VQFN、40)	6mm × 6mm

(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
(3) デバイスのプレビュー (量産データではありません)。



デバイスのブロック図

ADVANCE INFORMATION

Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Pin Configuration and Functions ... 3
5 Specifications ... 5
5.1 Absolute Maximum Ratings ... 5
5.2 ESD Ratings ... 5
5.3 Thermal Information ... 5
5.4 Recommended Operating Conditions ... 6
5.5 Electrical Characteristics ... 7
5.6 Timing Requirements ... 9
5.7 Switching Characteristics ... 10
5.8 Timing Diagrams ... 11
5.9 Typical Characteristics: All Devices ... 14
5.10 Typical Characteristics: ADS9219 ... 15
5.11 Typical Characteristics ... 16
5.12 Typical Characteristics: ADS9217 ... 17
6 Detailed Description ... 18
6.1 Overview ... 18
6.2 Functional Block Diagram ... 18
6.3 Feature Description ... 19
6.4 Device Functional Modes ... 27
6.5 Programming ... 29
7 Register Map ... 33
7.1 Register Bank 0 ... 33
7.2 Register Bank 1 ... 36
7.3 Register Bank 2 ... 54
8 Application and Implementation ... 56
8.1 Application Information ... 56
8.2 Typical Applications ... 56
8.3 Power Supply Recommendations ... 61
8.4 Layout ... 62
9 Device and Documentation Support ... 63
9.1 Documentation Support ... 63
9.2 ドキュメントの更新通知を受け取る方法 ... 63
9.3 サポート・リソース ... 63
9.4 Trademarks ... 63
9.5 静電気放電に関する注意事項 ... 63
9.6 用語集 ... 63
10 Revision History ... 63
11 Mechanical, Packaging, and Orderable Information ... 64
11.1 Mechanical Data ... 65

4 Pin Configuration and Functions

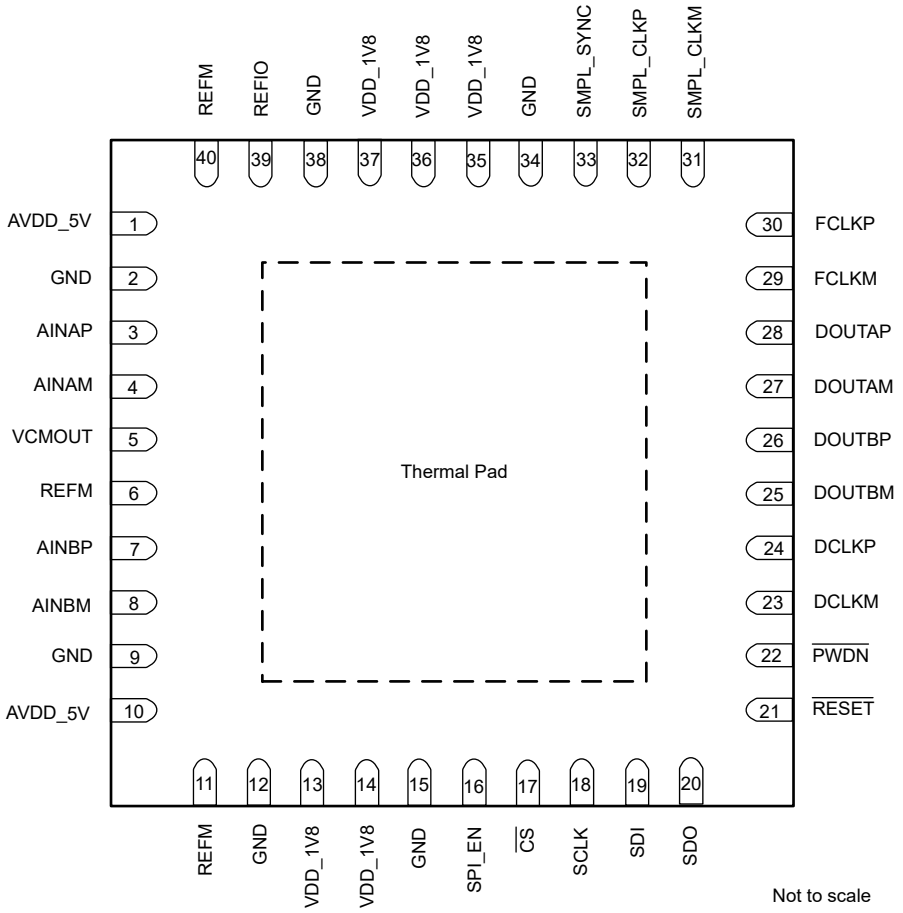


図 4-1. RHA Package, 6-mm × 6-mm, 40-Pin VQFN (Top View)

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
AINAM	4	I	Negative analog input for ADC A.
AINAP	3	I	Positive analog input for ADC A.
AINBM	8	I	Negative analog input for ADC B.
AINBP	7	I	Positive analog input for ADC B.
AVDD_5V	1, 10	P	5V analog power-supply pin.
$\overline{CS}$	17	I	Chip-select input pin for the configuration interface; active low.
DCLKM	23	O	Negative differential data clock output. Connect a 100Ω resistor between DCLKP and DCLKM close to the receiver.
DCLKP	24	O	Positive differential data clock output. Connect a 100Ω resistor between DCLKP and DCLKM close to the receiver.
DOUTAM	27	O	Negative differential data output. Connect a 100Ω resistor between DOUTAP and DOUTAM close to the receiver. Transmits ADC A data in 2-lane mode. Transmits ADC A and ADC B data in 1-lane mode.
DOUTAP	28	O	Positive differential data output corresponding to ADC A. Connect a 100Ω resistor between DOUTAP and DOUTAM close to the receiver. Transmits ADC A data in 2-lane mode. Transmits ADC A and ADC B data in 1-lane mode.

ADVANCE INFORMATION

ADVANCE INFORMATION

Pin Functions (続き)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
DOUTBM	25	O	Negative differential data output corresponding to ADC B in 2-lane mode. Connect a 100Ω resistor between DOUTBP and DOUTBM close to the receiver. Unused in 1-lane mode.
DOUTBP	26	O	Positive differential data output corresponding to ADC B in 2-lane mode. Connect a 100Ω resistor between DOUTBP and DOUTBM close to the receiver. Unused in 1-lane mode.
FCLKM	29	O	Negative differential data frame clock output. Connect a 100Ω resistor between FCLKP and FCLKM close to the receiver.
FCLKP	30	O	Positive differential data frame clock output. Connect a 100Ω resistor between FCLKP and FCLKM close to the receiver.
GND	2, 9, 12, 15, 34, 38	P	Ground.
$\overline{\text{PWDN}}$	22	I	Power-down control; active low. Connect to VDD_1V8 if unused.
REFIO	39	I/O	Internal reference voltage output. External reference voltage input. Connect a 10µF decoupling capacitor to REFM.
REFM	6, 11, 40	P	Reference ground. Connect to GND.
$\overline{\text{RESET}}$	21	I	Reset input; active low. Connect to VDD_1V8 if unused.
SCLK	18	I	Serial clock input for the configuration interface.
SDI / $\overline{\text{EXTREF}}$	19	I	SDI is a multifunction logic input; pin function is determined by the SPI_EN pin. SDI has an internal 100kΩ pulldown resistor to GND. SPI_EN = 0b: SDI is the logic input to select between the internal or external reference. Connect SDI to GND for the external reference. Connect SDI to IOVDD for the internal reference. SPI_EN = 1b: Serial data input for the configuration interface
SDO	20	O	Serial data output for the configuration interface.
SMPL_CLKM	31	I	ADC sampling clock input. Negative differential input for the LVDS sampling clock. Connect this pin to GND for the CMOS sampling clock.
SMPL_CLKP	32	I	ADC sampling clock input. Positive differential input for the LVDS sampling clock. Clock input for the CMOS sampling clock.
SMPL_SYNC	33	I	Synchronization input for internal averaging filter. Connect to GND if unused. See the *Synchronizing Multiple ADCs* section on how to use the SMPL_SYNC pin.
SPI_EN	16	I	Control to enable configuration of the SPI interface; active high. Connect a pullup resistor to VDD_1V8 to keep the configuration interface enabled. Connect to GND if SPI configuration is unused.
Thermal Pad	—	P	Exposed thermal pad. Connect to GND.
VCMOUT	5	O	Common-mode voltage output. Use VCMOUT to set the common-mode voltage at the ADC inputs. Connect a 1µF decoupling capacitor to GND.
VDD_1V8	13, 14, 35, 36, 37	P	1.8V power-supply. Connect 1µF and 0.1µF decoupling capacitors to GND.

(1) I = input, O = output, I/O = input or output, G = ground, P = power.

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
VDD_1V8 to GND	–0.3	2.1	V
AVDD_5V to GND	–0.3	5.5	V
AINAP, AINAM, AINBP, and AINBM to GND	GND – 0.3	AVDD_5V + 0.3	V
REFIO to REFM	REFM – 0.3	AVDD_5V + 0.3	V
Digital inputs to GND	GND – 0.3	VDD_1V8 + 0.3	V
REFM to GND	–0.3	0.3	V
Input current to any pin except supply pins(2)	–10	10	mA
Junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–60	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Pin current must be limited to 10 mA or less.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, analog input pins AINAP, AINAM, AINBP, and AINBM(1)	±2000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all other pins(1)	±1000	
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Thermal Information

THERMAL METRIC(1)		ADS921x RHA (VQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	7.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

ADVANCE INFORMATION

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
AVDD_5V	Analog power supply AVDD_5V to GND	ADS9217	4.5	5	5.5	V
		ADS9218, ADS9219	4.75	5	5.25	
VDD_1V8	Power supply	VDD_1V8 to GND	1.75	1.8	1.85	V
REFERENCE VOLTAGE						
V_{REF}	Reference voltage to the ADC	External reference	4.076	4.096	4.116	V
ANALOG INPUTS						
V_{IN}	Absolute input voltage	AINx(1) to GND	V_{CM} – 1.6		V_{CM} + 1.6	V
FSR	Full-scale input range	(AINAP – AINAM) and (AINBP – AINBM)	–3.2		3.2	V
V_{CM}	Common-mode input range	(AINAP + AINAM) / 2 and (AINBP + AINBM) / 2	V_{CMOUT} – 0.05		V_{CMOUT} + 0.05	V
TEMPERATURE RANGE						
T_A	Ambient temperature		–40	25	125	°C

(1) AINx refers to analog inputs AINAP, AINAM, AINBP, and AINBM.

ADVANCE INFORMATION

5.5 Electrical Characteristics

at AVDD_5V = 4.75V to 5.25V for ADS9219, and ADS9218, and AVDD_5V = 4.5V to 5.5V for ADS9217 , VDD_1V8 = 1.75V to 1.85V, internal V_{REF} = 4.096V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
I_B	Input bias current			0.5	TBD	µA
	Input bias current thermal drift			1		nA/℃
DC PERFORMANCE						
	Resolution	No missing codes		18		Bits
DNL	Differential nonlinearity		–0.75	±0.4	0.75	LSB
INL	Integral nonlinearity	T_A = 0°C to 70°C, ADS9217 and ADS9218	–1.5	±0.8	1.5	LSB
			–5.7	±3	5.7	ppm
		T_A = –40°C to 125°C, ADS9217 and ADS9218	–2	±0.8	2	LSB
			–7.6	±3	7.6	ppm
		ADS9219 at 20MSPS	TBD	±1	TBD	LSB
			TBD	±3.8	TBD	ppm
		ADS9219 up to 16MSPS	TBD	±0.8	TBD	LSB
			TBD	±3.8	TBD	ppm
$V_{(OS)}$	Input offset error			±20		LSB
dV_{OS}/dT	Input offset error thermal drift			±0.5	1.5	ppm/°C
G_E	Gain error(1)		–0.05	±0.01	0.05	%FSR
dG_E/dT	Gain error thermal drift(1)			±1	2	ppm/°C
AC PERFORMANCE						
SINAD	Signal-to-noise + distortion ratio	f_{IN} = 2kHz		95		dB
		f_{IN} = 1MHz		94		
SNR	Signal-to-noise ratio	f_{IN} = 2kHz		95.5		dB
		f_{IN} = 1MHz		94.9		
THD	Total harmonic distortion	f_{IN} = 2kHz, ADS9217 and ADS9218		–118		dB
		f_{IN} = 2kHz, ADS9219 at 20MSPS		–110		
		f_{IN} = 2kHz, ADS9219 up to 16MSPS		–118		
		f_{IN} = 1MHz, all devices		–104		
SFDR	Spurious-free dynamic range	f_{IN} = 2kHz		120		dB
		f_{IN} = 1MHz		104		
	Isolation crosstalk	f_{IN} = 2kHz		TBD		dB
	Aperture jitter			0.3		ps_{RMS}
BW	Input Bandwidth (–3dB)	ADS9219		135		MHz
		ADS9218		90		
		ADS9217		45		
COMMON-MODE OUTPUT BUFFER						
V_{CMOUT}	Common-mode output voltage		2.2	2.4	2.65	V
	Output current drive		0		5	µA
LVDS RECEIVER (SMPL_CLK)						
V_{TH}	High-level input voltage (P – M)	AC coupled	300			mV
		DC coupled	100			
V_{TL}	Low-level input voltage (P – M)	AC coupled			–300	mV
		DC coupled			–100	

ADVANCE INFORMATION

5.5 Electrical Characteristics (続き)

at AVDD_5V = 4.75V to 5.25V for ADS9219, and ADS9218, and AVDD_5V = 4.5V to 5.5V for ADS9217 , VDD_1V8 = 1.75V to 1.85V, internal V_{REF} = 4.096V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ICM}	Input common-mode voltage		0.5	1.2	1.4	V
LVDS OUTPUT (CLKOUT, DOUTA, and DOUTB)						
V_{ODIFF}	Differential output voltage	R_L = 100Ω	TBD	350	TBD	mV
V_{OCM}	Output common-mode voltage	R_L = 100Ω	1.08	1.1	1.32	V
CMOS INPUTS ($\overline{CS}$, SCLK, and SDI)						
V_{IL}	Input low logic level		–0.1		0.5	V
V_{IH}	Input high logic level		1.3		VDD_1V8	V
CMOS OUTPUT (SDO)						
V_{OL}	Output low logic level	I_{OL} = 200µA sink	0		0.4	V
V_{OH}	Output high logic level	I_{OH} = 200µA source	1.4		VDD_1V8	V
POWER SUPPLY						
I_{AVDD_5V}	Supply current from AVDD_5V	At 20MSPS throughput (ADS9219)		38.2	50	mA
		At 10MSPS throughput (ADS9218)		31.2	40	
		At 5MSPS throughput (ADS9217)		18.5	24	
		Power-down			2	
I_{VDD_1V8}	Supply current from VDD_1V8	At 20MSPS throughput (ADS9219)		85.3	97	mA
		At 10MSPS throughput (ADS9218)		69.8	89	
		At 5MSPS throughput (ADS9217)		48.8	66	
		Power-down			2	

(1) These specifications include full temperature range variation but not the error contribution from internal reference.

ADVANCE INFORMATION

5.6 Timing Requirements

at AVDD_5V = 4.75V to 5.25V for ADS9219, and ADS9218, and AVDD_5V = 4.5V to 5.5V for ADS9217 , VDD_1V8 = 1.75V to 1.85V, internal V_{REF} = 4.096V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

			MIN	MAX	UNIT
CONVERSION CYCLE					
f_{CYCLE}	Sampling frequency	ADS9219		20	MHz
		ADS9218	3.6	10	
		ADS9217	3.6	5	
t_{CYCLE}	ADC cycle time period		1 / f_{CYCLE}		s
$t_{PL\_SMPLCLK}$	Sample clock low time		0.48	0.52	t_{CYCLE}
$t_{PH\_SMPLCLK}$	Sample clock high time		0.48	0.52	t_{CYCLE}
f_{CLK}	Maximum SCLK frequency			10	MHz
t_{CLK}	Minimum SCLK time period		100		ns
SPI TIMINGS					
t_{hi_CSZ}	Pulse duration: $\overline{CS}$ high		220		ns
t_{PH_CK}	SCLK high time		0.48	0.52	t_{CLK}
t_{PL_CK}	SCLK low time		0.48	0.52	t_{CLK}
t_{d_CSCK}	Setup time: $\overline{CS}$ falling to the first SCLK rising edge		20		ns
t_{su_CKDI}	Setup time: SDI data valid to the corresponding SCLK rising edge		10		ns
t_{ht_CKDI}	Hold time: SCLK rising edge to corresponding data valid on SDI		5		ns
t_{d_CKCS}	Delay time: last SCLK falling edge to $\overline{CS}$ rising		5		ns

ADVANCE INFORMATION

5.7 Switching Characteristics

at AVDD_5V = 4.75V to 5.25V for ADS9219, and ADS9218, and AVDD_5V = 4.5V to 5.5V for ADS9217 , VDD_1V8 = 1.75V to 1.85V, internal V_{REF} = 4.096V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
RESET					
t_{PU}	Power-up time for device			25	ms
LVDS DATA INTERFACE					
t_{RT}	Rise time	With 50Ω transmission line of length = 20mm, differential R_L = 100Ω, and C_L = 1pF		600	ps
t_{FT}	Fall time			600	ps
t_{CYCLE}	Sampling clock period	ADS9219	50		ns
		ADS9218	100		
		ADS9217	200		
t_{DCLK}	Clock output		4.167		ns
	Clock duty cycle		45	55	%
t_{d_DCLKDO}	Time delay: DCLKP rising to corresponding data valid	At 5MSPS, SDR mode	–0.8	0.8	ns
$t_{off\_DCLKDO\_r}$	Time offset: DCLKP rising to corresponding data valid	At 5MSPS, DDR mode	t_{DCLK} / 4 – 0.8	t_{DCLK} / 4 + 0.8	ns
$t_{off\_DCLKDO\_f}$	Time offset: DCLKP falling to corresponding data valid	At 5MSPS, DDR mode	t_{DCLK} / 4 – 0.8	t_{DCLK} / 4 + 0.8	ns
t_{PD}	Time delay: SMPL_CLK falling to DCLKP rising			t_{DCLK}	ns
$t_{PU\_SMPL\_CLK}$	Time delay: Free-running clock connected to SMPL_CLK to ADC data valid			100	µs
SPI TIMINGS					
t_{den_CKDO}	Time delay: 8th SCLK rising edge to SDO enable			30	ns
t_{dz_CKDO}	Time delay: 24th SCLK rising edge to SDO going Hi-Z			30	ns
t_{d_CKDO}	Time delay: SCLK launch edge to corresponding data valid on SDO			20	ns
t_{ht_CKDO}	Hold time: SCLK launch edge to previous data valid on SDO		2		ns

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5.8 Timing Diagrams

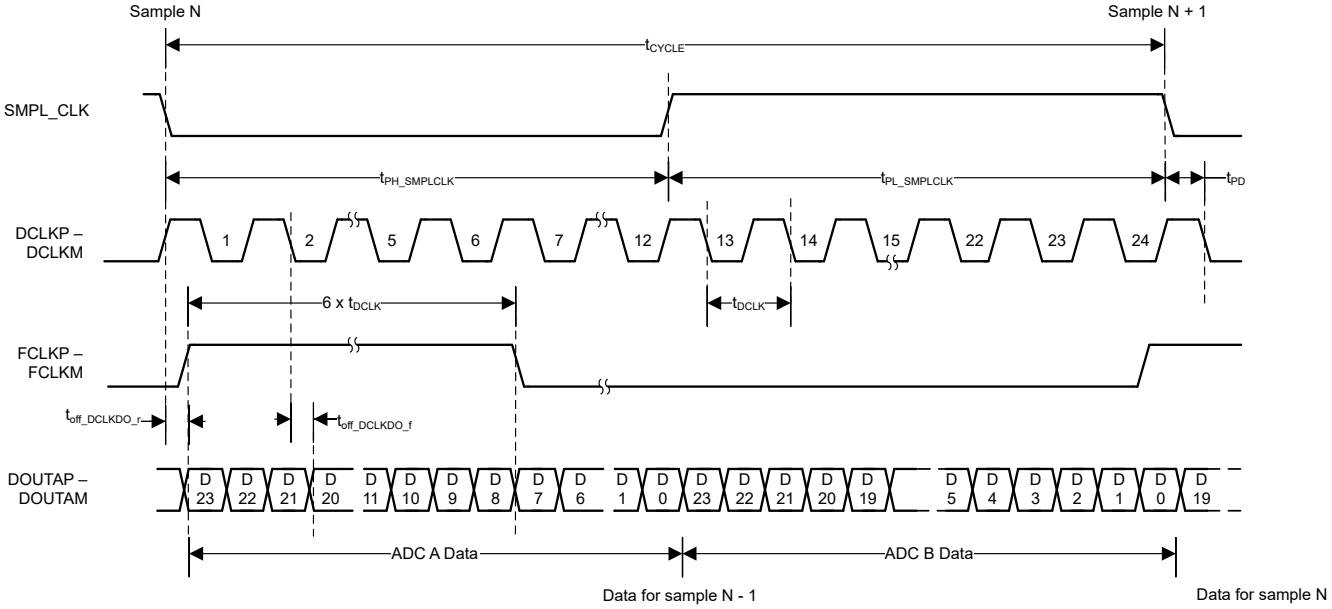


図 5-1. LVDS Data Interface: 1-Lane DDR

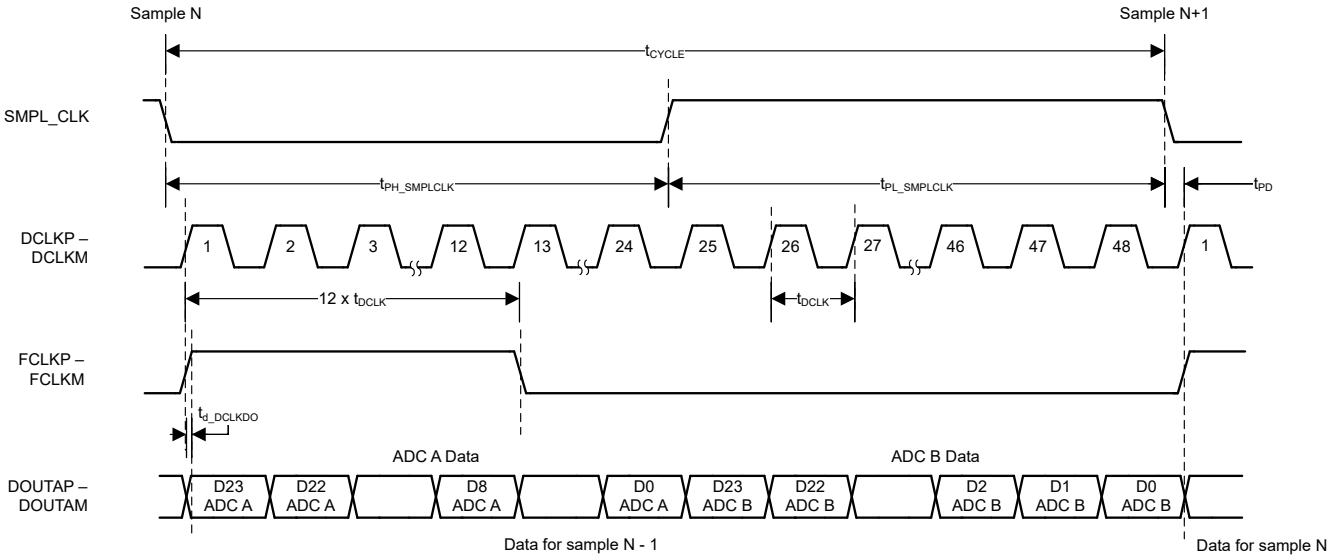


図 5-2. LVDS Data Interface: 1-Lane SDR

ADVANCE INFORMATION

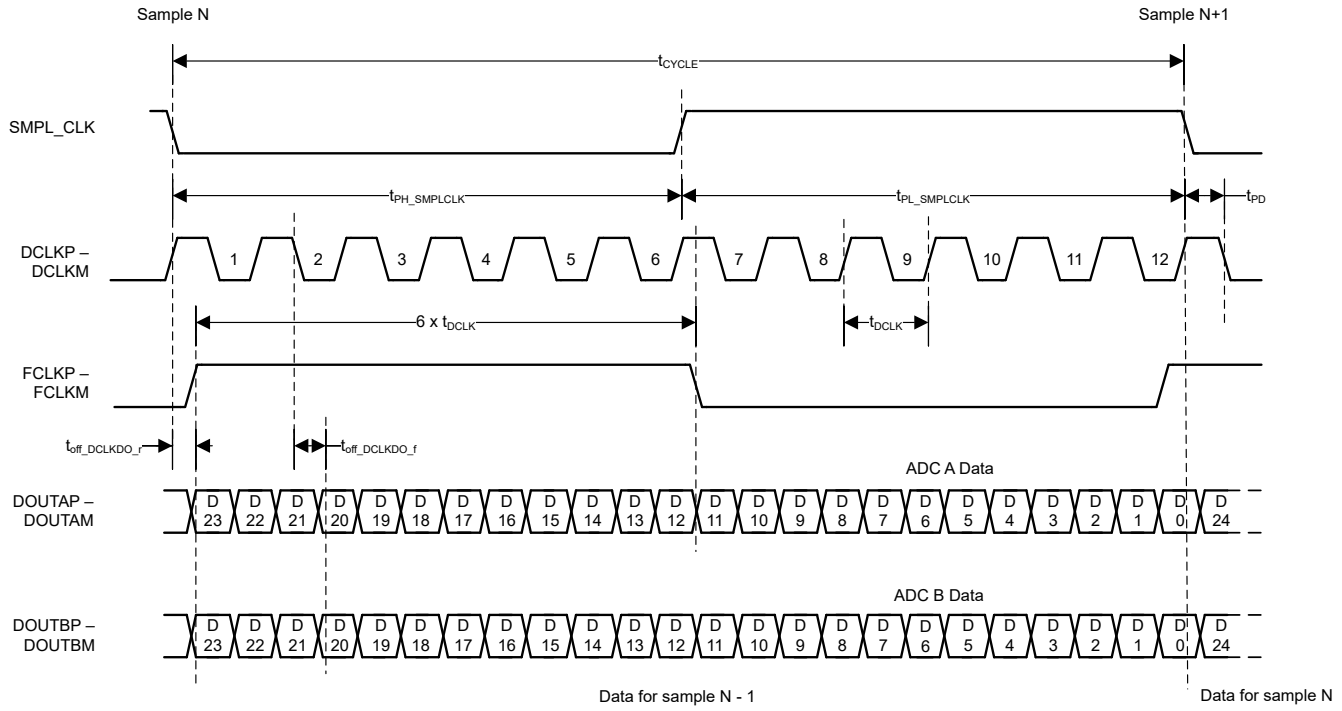


図 5-3. LVDS Data Interface: 2-Lane DDR

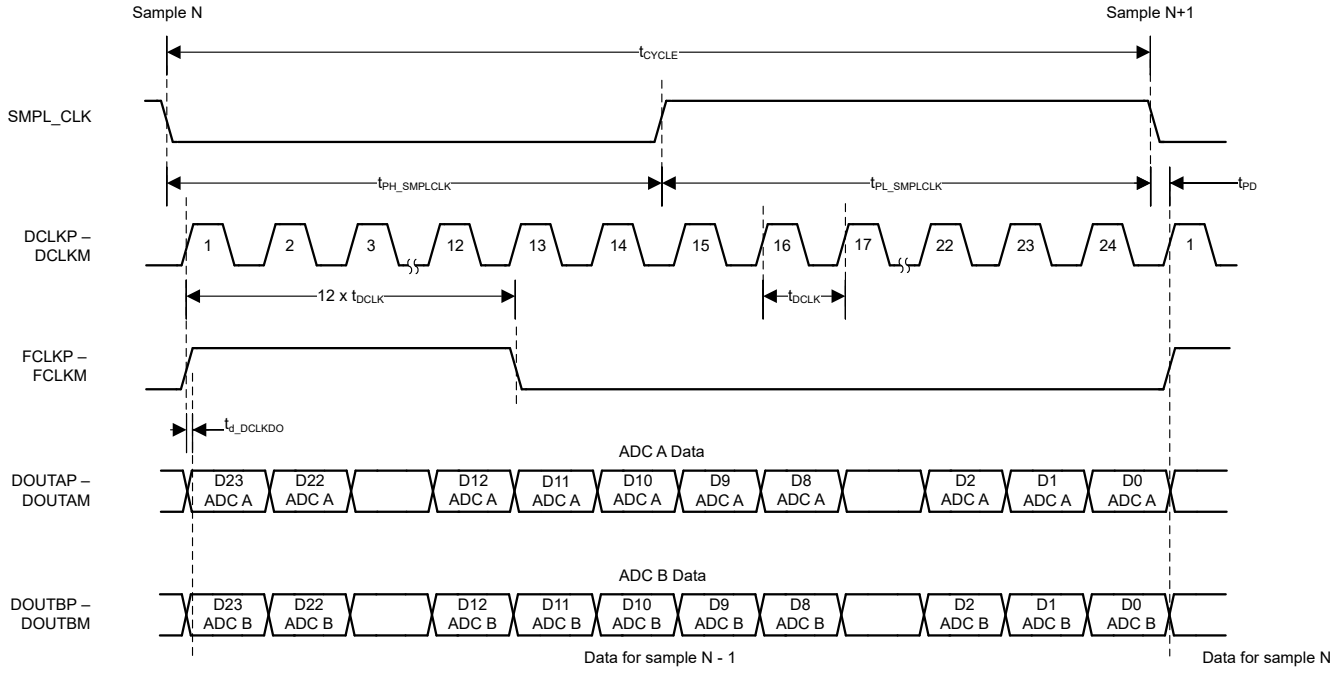


図 5-4. LVDS Data Interface: 2-Lane SDR

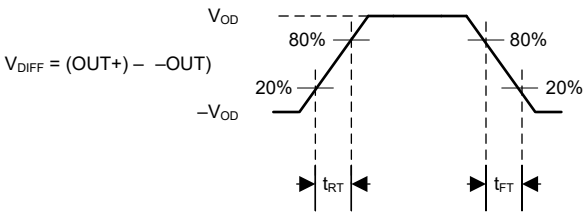


図 5-5. LVDS Output Transition Times

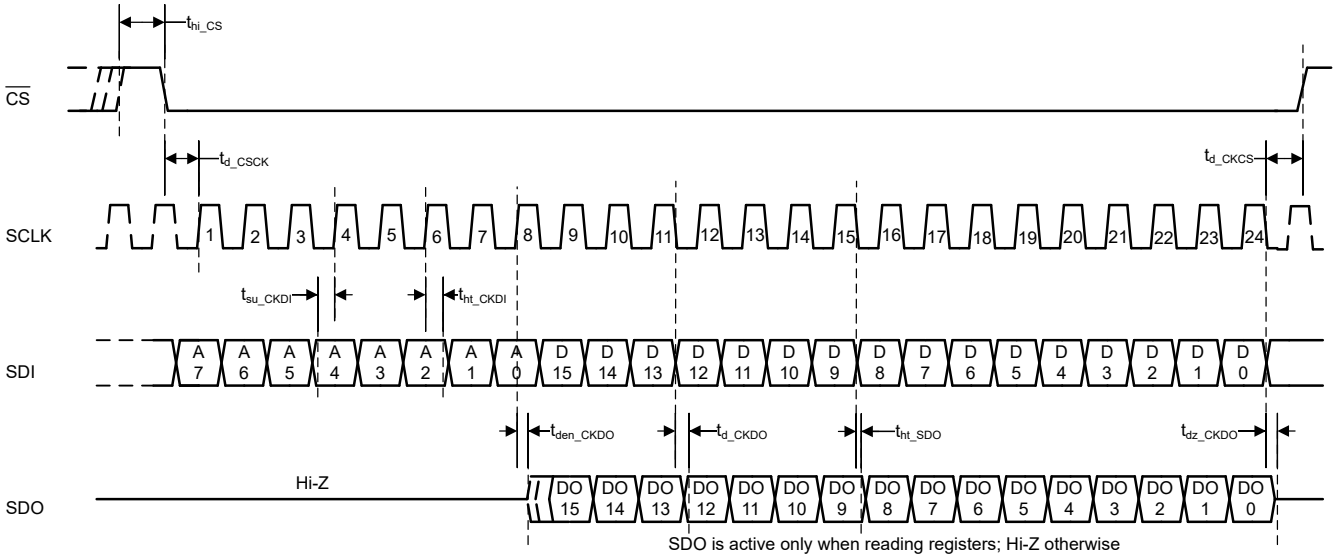


図 5-6. Configuration SPI

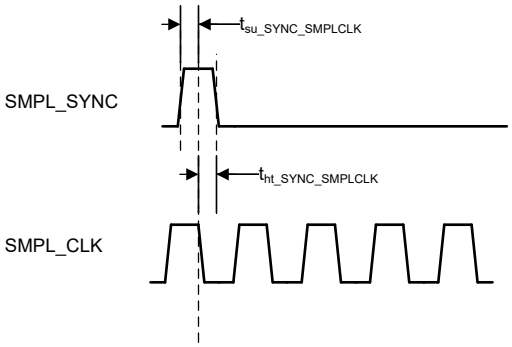


図 5-7. SMPL_SYNC Timing

ADVANCE INFORMATION

5.9 Typical Characteristics: All Devices

at T_A = 25°C, AVDD_5V = 5V, VDD_1V8 = 1.8V, external V_{REF} = 4.096V, and maximum throughput (unless otherwise noted)

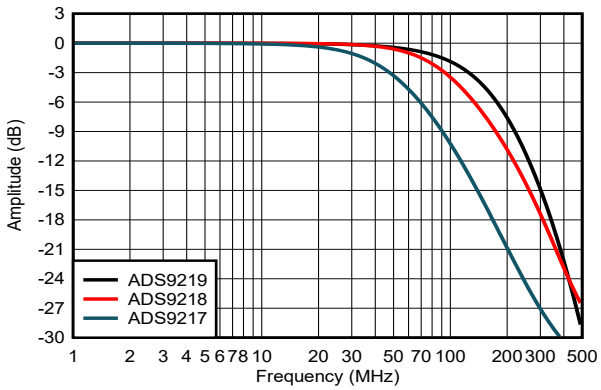
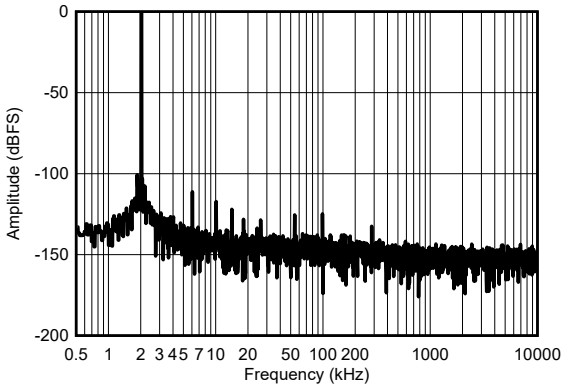


図 5-8. Typical Analog Input Bandwidth

ADVANCE INFORMATION

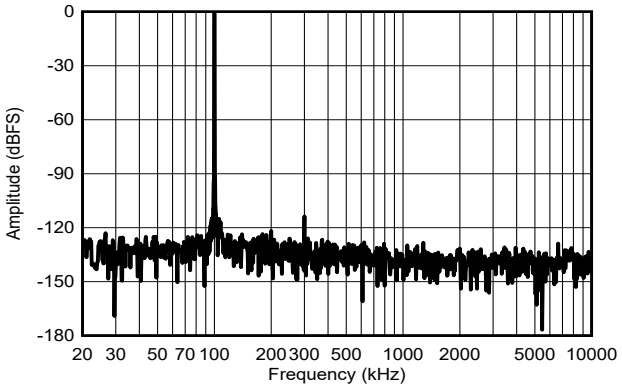
5.10 Typical Characteristics: ADS9219

at T_A = 25°C, AVDD_5V = 5V, VDD_1V8 = 1.8V, external V_{REF} = 4.096V, and maximum throughput (unless otherwise noted)



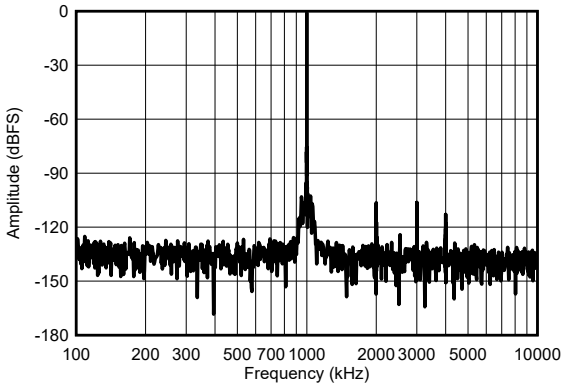
f_{IN} = 2kHz, SNR = 95.5dBFS, THD = –111.5dB

図 5-9. Typical FFT for f_{IN} = 2kHz



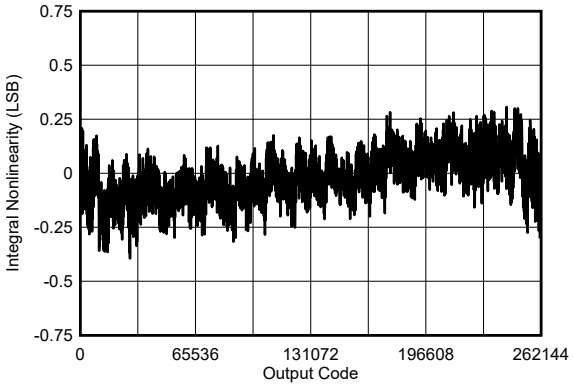
f_{IN} = 100kHz, SNR = 95.4dBFS, THD = –111.6dB

図 5-10. Typical FFT for f_{IN} = 100kHz



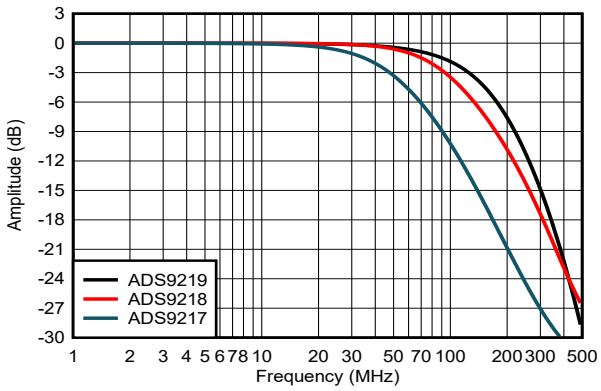
f_{IN} = 1MHz, SNR = 94.9dBFS, THD = –104.2dB

図 5-11. Typical FFT for f_{IN} = 1MHz



Typical INL = ±0.4LSB

図 5-12. Typical INL



Typical BW (–3dB) = 90MHz

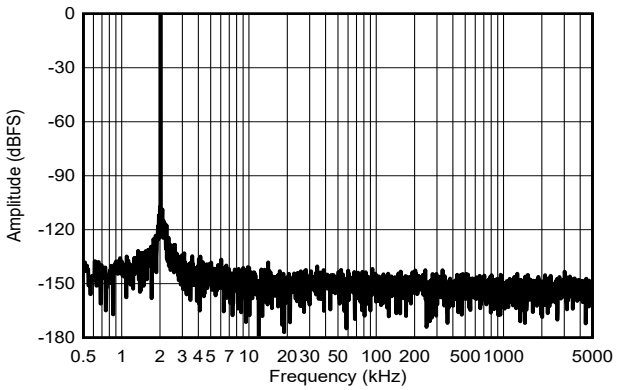
図 5-13. Typical Analog Input Bandwidth

ADVANCE INFORMATION

ADVANCE INFORMATION

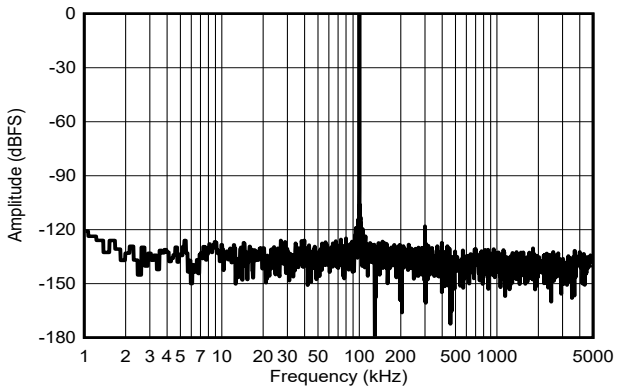
5.11 Typical Characteristics

at T_A = 25°C, AVDD_5V = 5V, VDD_1V8 = 1.8V, external V_{REF} = 4.096V, and maximum throughput (unless otherwise noted)



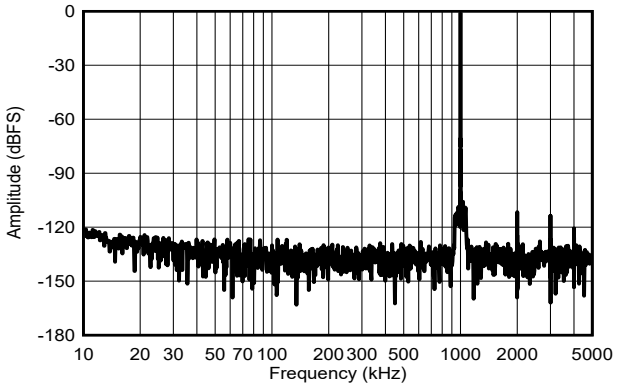
f_{IN} = 2kHz, SNR = 95.5dB, THD = -120dB

図 5-14. Typical FFT for f_{IN} = 2kHz



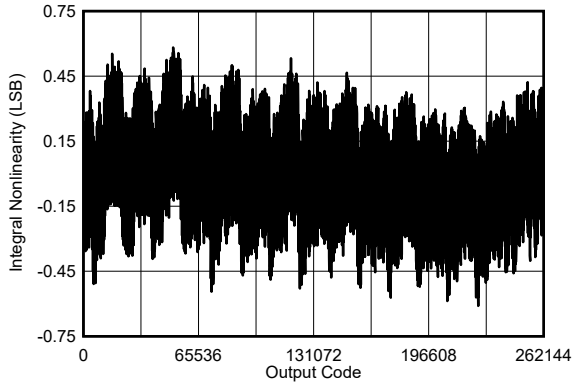
f_{IN} = 100kHz, SNR = 95.5dBFS, THD = –118.2dB

図 5-15. Typical FFT for f_{IN} = 100kHz



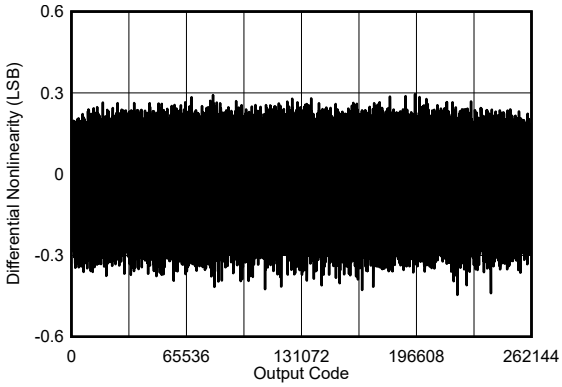
f_{IN} = 1MHz, SNR = 95dBFS, THD = –106dB

図 5-16. Typical FFT for f_{IN} = 1MHz



Typical INL = ±0.6LSB

図 5-17. Typical INL

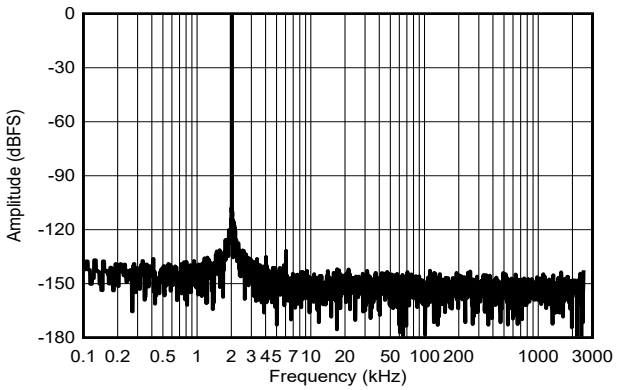


Typical DNL = ±0.4LSB

図 5-18. Typical DNL

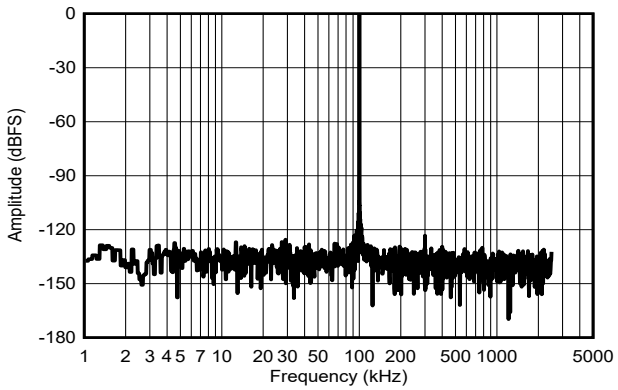
5.12 Typical Characteristics: ADS9217

at T_A = 25°C, AVDD_5V = 5V, VDD_1V8 = 1.8V, external V_{REF} = 4.096V, and maximum throughput (unless otherwise noted)



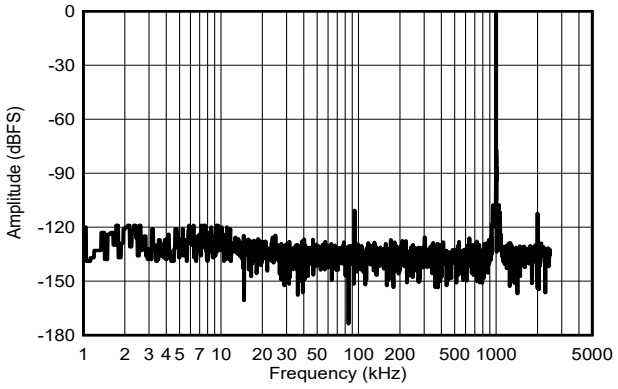
f_{IN} = 2kHz, SNR = 95.5dBFS, THD = –120dB

図 5-19. Typical FFT for f_{IN} = 2kHz



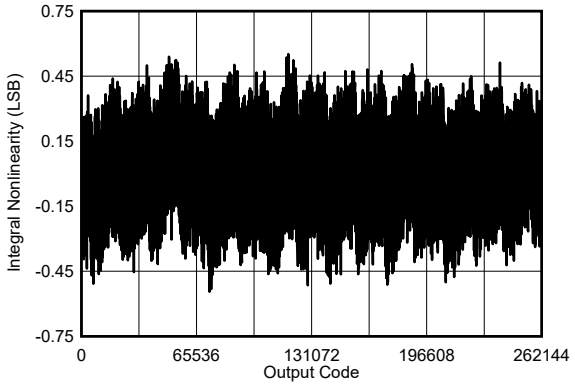
f_{IN} = 100kHz, SNR = 95.4dBFS, THD = –120dB

図 5-20. Typical FFT for f_{IN} = 100kHz



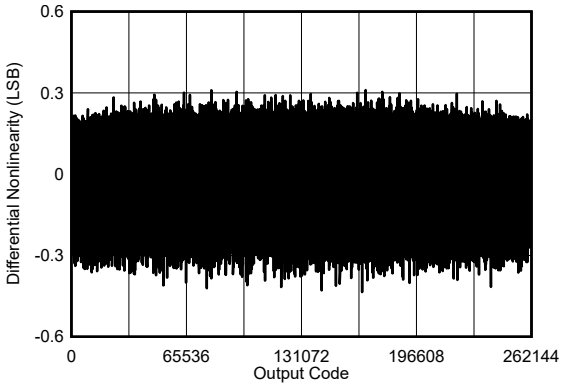
f_{IN} = 1MHz, SNR = 94.9dBFS, THD = –103.5dB

図 5-21. Typical FFT for f_{IN} = 1MHz



Typical INL = ±0.6LSB

図 5-22. Typical INL



Typical DNL = ±0.4LSB

図 5-23. Typical DNL

ADVANCE INFORMATION

ADVANCE INFORMATION

6 Detailed Description

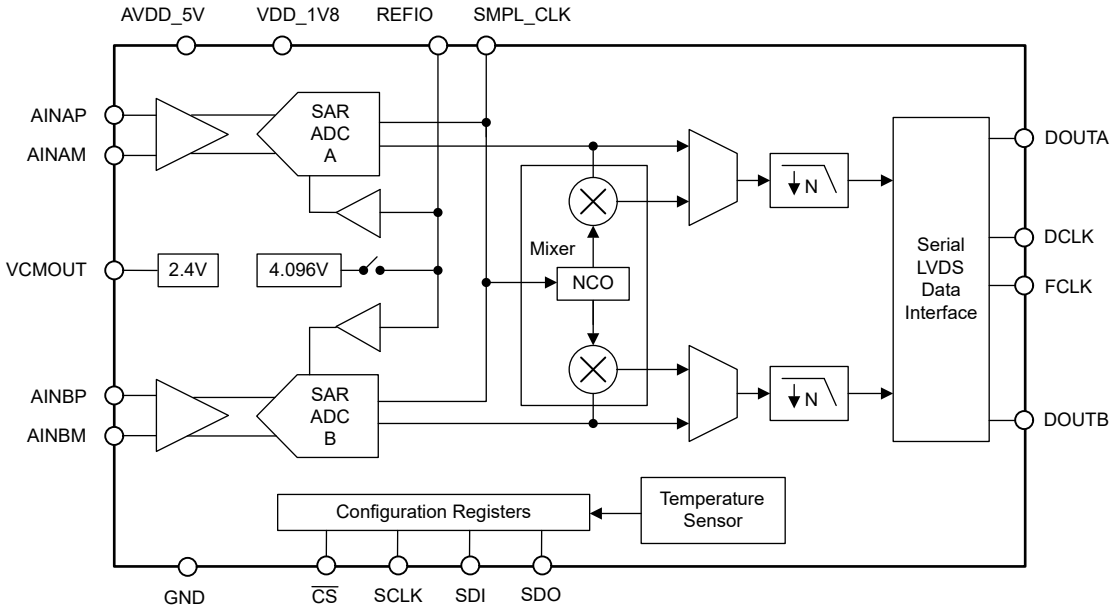
6.1 Overview

The ADS921x is an 18 ビット, 20MSPS/ch, dual-channel, simultaneous-sampling, analog-to-digital converter (ADC). The ADS921x integrates a high-impedance buffer at the ADC inputs, voltage reference, reference buffer, and common-mode voltage output buffer. The ADS9219 supports unipolar differential analog input signals. The buffer at the ADC inputs is optimized for low-distortion and low-power operation.

For DC level shifting of the analog input signals, the device has a common-mode voltage output buffer. The common-mode voltage is derived from the output of the integrated reference buffer. When a conversion is initiated, the differential input between the (AINAP – AINAM) and (AINBP – AINBM) pins is sampled. The ADS921x uses a clock input on the SMPL_CLKP pin to initiate conversions.

The ADS921x consumes only 172mW/チャネル of power when operating at 20MSPS/チャネル, which includes the buffer power dissipation at the ADC inputs. The serial LVDS (SLVDS) digital interface simplifies board layout, timing, firmware, and supports full throughput at lower clock speeds.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Analog Inputs

The ADS921x supports both AC-coupled and DC-coupled differential analog inputs. Make sure the input common-mode voltage of the analog inputs matches the voltage level on the VCMOUT pin. 図 6-1 shows the equivalent input network diagram of the device.

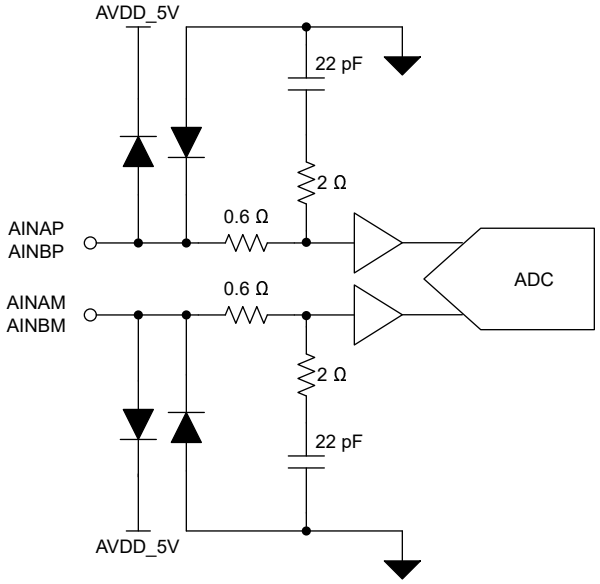


図 6-1. Equivalent Input Network

6.3.2 Analog Input Bandwidth

図 5-8 illustrates the analog full-power input bandwidth of the ADS921x device family. The –3dB bandwidth is 135MHz, 90MHz, and 45MHz for the ADS9219, ADS9218, and ADS9217, respectively.

6.3.3 ADC Transfer Function

The ADS921x supports a ±3.2V differential input range. The device outputs 18 ビット conversion data in either straight-binary or binary two's-complement formats. As shown in 表 6-1, the format for the output codes is the same across all analog channels. Configure the format for the output codes with the DATA_FORMAT field in register address 0x0D. The least significant bit (LSB) for the ADC is given by 1LSB = 6.4V / 2^{18} .

表 6-1. Transfer Characteristics

INPUT VOLTAGE	DESCRIPTION	ADC OUTPUT IN 2's-COMPLEMENT FORMAT	ADC OUTPUT IN STRAIGHT-BINARY FORMAT
≤ –3.2V + 1LSB	Negative full-scale code	0x80000	0x00000
0V + 1LSB	Mid-code	0x00000	0x1FFFF
≥ 3.2V – 1LSB	Positive full-scale code	0x1FFFF	0x3FFFF

ADVANCE INFORMATION

6.3.4 Reference Voltage

The ADS921x has a precision, low-drift voltage reference internal to the device. For best performance, the internal reference noise is filtered (as shown in 図 6-2) by connecting a 10µF ceramic bypass capacitor to the REFIO pin. As shown in 図 6-3, an external reference is also connected at the REFIO pin. When using an external reference, disable the internal reference voltage by writing PD_REF = 1b in address 0xC1 of register bank 1.

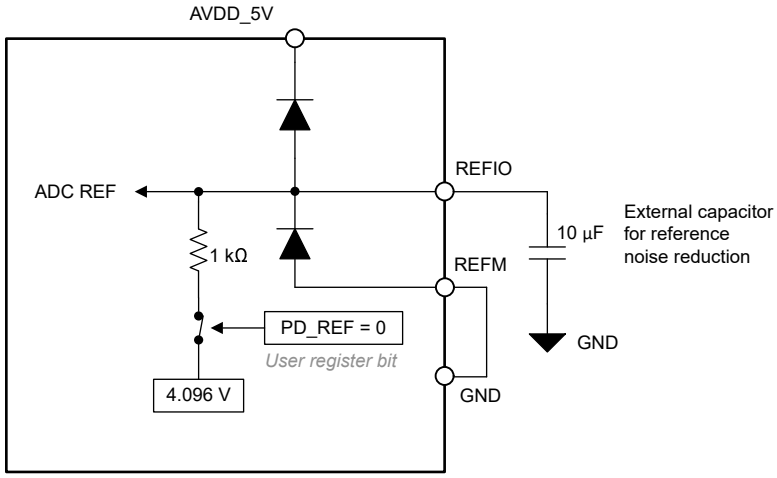


図 6-2. Internal Reference Voltage

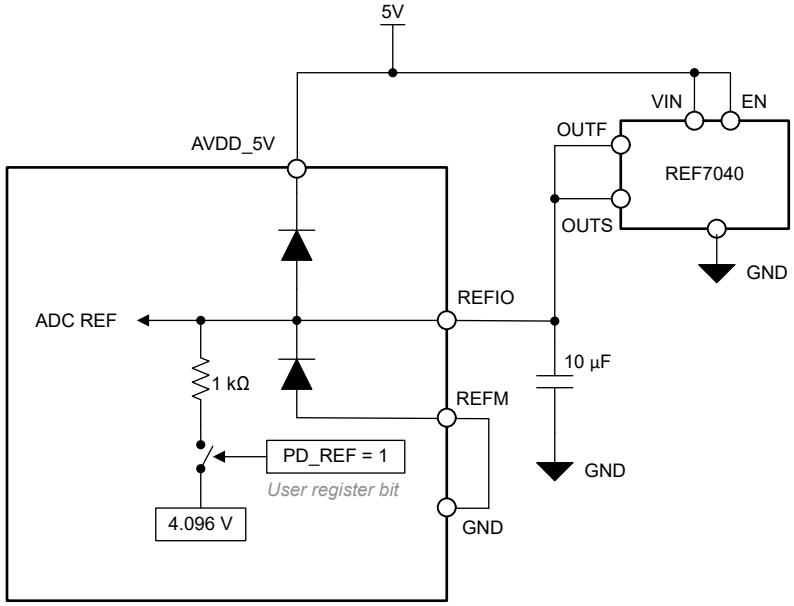


図 6-3. External Reference Voltage

6.3.5 Temperature Sensor

The ADS921x features a 10-bit temperature sensor for measuring temperature inside the device. Follow the sequence listed in 表 6-2 to read the temperature sensor output with the SPI. Read the temperature sensor data at anytime independent of the ADC data interface.

The transfer function for the temperature sensor is given by 式 1:

$$\text{Temperature} = -85.0172 + (10\text{ bit output} \times 0.24918)\ ^{\circ}\text{C} \quad (1)$$

表 6-2. Sequence to Read Temperature Sensor Output

REGISTER ADDRESS	REGISTER BANK	VALUE	COMMENT
0x90	1	0x4000	Write register to load temperature sensor output in address 0x91
0x91	1	10 bit temperature sensor data	Read register for temperature sensor output
0x90	1	0x0000	Write register

6.3.6 Data Averaging

The ADS921x features a built-in decimation filter that averages the conversion results from the ADC. The output data rate is reduced with higher data averaging. 表 6-3 shows the register settings corresponding to oversampling ratios.

As shown in 図 6-4, a pulse on the SMPL_SYNC pin resets the decimation filter. A pulse on SMPL_SYNC synchronizes multiple ADS921x devices when using the decimation filter.

表 6-3. Register Map Settings for OSR

DECIMATION	REGISTER	VALUE
OSR initialization	CLK3 (0xC5[9])	1
	OSR_INIT1 (0xC0[11:10])	0 for DATA_LANES = 5 or 7 1 for DATA_LANES = 0 or 2
	OSR_INIT2 (0xC4[5:4])	2
	OSR_INIT3 (0xC4[1])	1
	OSR_EN (0x0D[6])	1
2	OSR (0x0D[5:2])	0
	OSR_CLK (0xC0[9:7])	0
4	OSR (0x0D[5:2])	1
	OSR_CLK (0xC0[9:7])	4
8	OSR (0x0D[5:2])	2
	OSR_CLK (0xC0[9:7])	5
16	OSR (0x0D[5:2])	3
	OSR_CLK (0xC0[9:7])	6

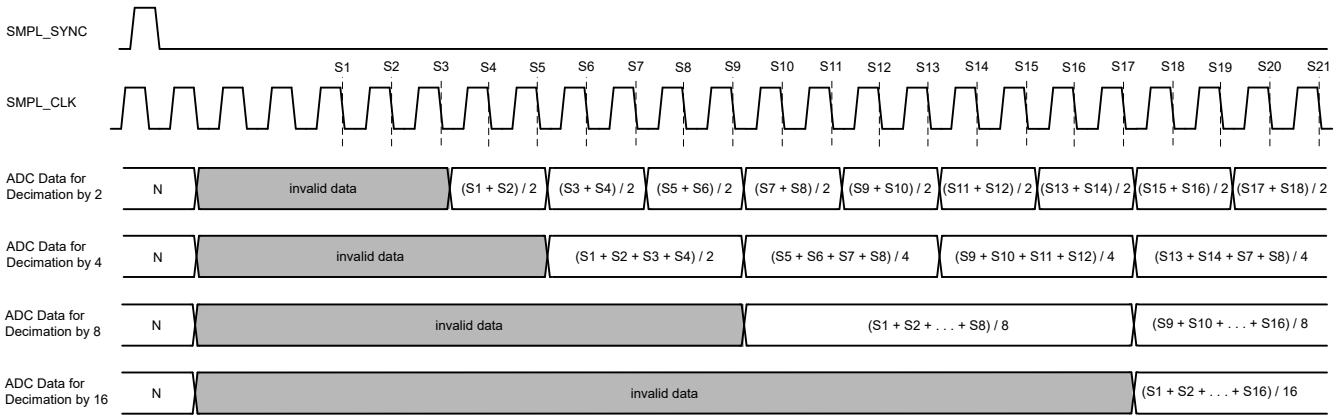


図 6-4. Data Output With Decimation

ADVANCE INFORMATION

ADVANCE INFORMATION

6.3.7 Digital Down Converter

The ADS921x includes an optional on-chip digital down conversion (DDC) that is enabled by SPI register settings. As shown in 図 6-5, the DDC includes a digital mixer and a 24-bit, numerically controlled oscillator (NCO). The digital mixer generates 24-bit I and Q outputs that represent complex mixing of ADC output data with the NCO output frequency. Each channel of the ADC generates a 48-bit output corresponding to the 24-bit I and Q outputs, respectively, from the digital mixer.

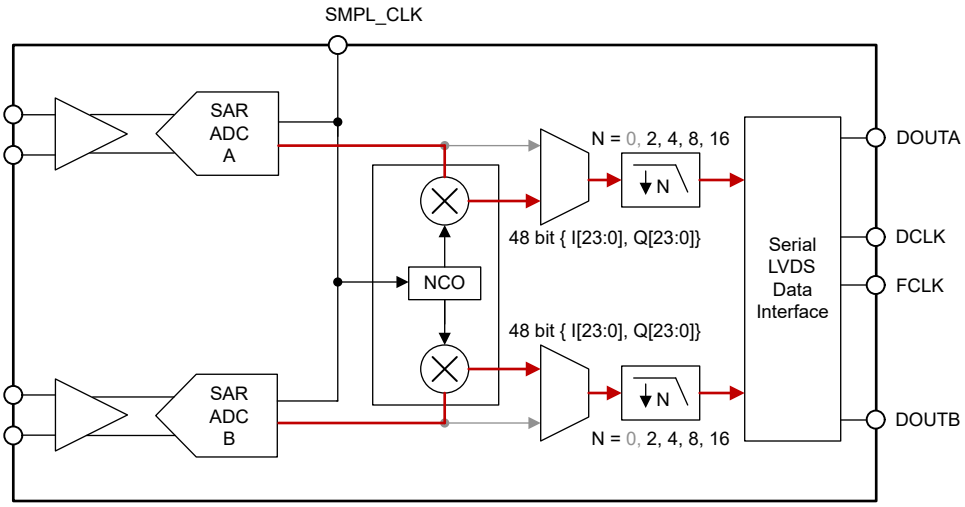


図 6-5. Data Path When Using a Digital Down Converter

The NCO is common for both ADC A and ADC B. The output frequency of the NCO, given by 式 2, is configured using the NCO_FREQUENCY register (address 0xFD and 0xFE).

$$f_{NCO} = \frac{f_{SMPL\_CLK}}{2^{24}} \times (NCO\_FREQUENCY[23:0] \,\&\, 0xFFFFF0)\ Hz \quad (2)$$

The output phase of the NCO is reset by applying a pulse on the SMPL_SYNC pin as shown in 図 5-7. As shown in 式 3 and 表 6-4, the initial phase of the NCO output is configured using the NCO_PHASE register (address 0xFC and 0xFD).

$$NCO\_PHASE[23:0] = \left(\frac{\text{Initial phase}}{2\pi} \times 2^{24}\right) \& \ 0xFFFFF0 \quad (3)$$

表 6-4. Initial NCO Phase

NCO_PHASE[23:0]	INITIAL PHASE
0x000000	0
0x7FFFF0	π
0xFFFFF0	2π

Use a decimation factor of either 2, 4, 8, or 16 with the DDC. 表 6-5 shows the register configuration for decimating the DDC output.

表 6-5. Decimation Settings for the DDC

DECIMATION	REGISTER	VALUE
2	OSR_EN (0x0D[6])	1
	OSR (0x0D[5:2]	0
	OSR_CLK (0xC0[9:7])	0
Common settings for decimation factors 4, 8, and 16	CLK3 (0xC5[9])	1
	OSR_INIT1 (0xC0[11:10])	1
	OSR_INIT2 (0xC4[5:4])	2
	OSR_INIT3 (0xC4[1])	1
	OSR_EN (0x0D[6])	1
4	OSR (0x0D[5:2]	1
	OSR_CLK (0xC0[9:7])	0
8	OSR (0x0D[5:2]	2
	OSR_CLK (0xC0[9:7])	4
16	OSR (0x0D[5:2]	3
	OSR_CLK (0xC0[9:7])	5

6.3.8 Data Interface

The ADS921x features a high-speed, serial LVDS data interface with 2-lane and 1-lane options for data output. The host configures the output data frame width to 20 bits or 24 bits with the single-data rate (SDR) and double-data rate (DDR) modes. 表 6-6 lists the register settings for this configuration.

表 6-6. Register Map Settings for Output Data Interface

DATA FRAME WIDTH (Bits)	DATA RATE	OUTPUT LANES	DATA_LANES 0x12[2:0]	DATA_RATE 0xC1[8]	CLK1 0xC0[12]	CLK2 0xC1[0]	CLK3 0xC5[9]
20	SDR	1	5	1	1	1	1
20	SDR	2	0	1	0	1	0
20	DDR	1	5	0	1	1	1
20	DDR	2	0	0	0	1	0
24	SDR	1	7	1	1	0	1
24	SDR	2	2	1	0	0	0
24	DDR	1	7	0	1	0	1
24	DDR	2	2	0	0	0	0

The ADS921x generates a data clock DCLK that is a multiple of the ADC sampling clock SMPL_CLK. The data clock frequency depends on the number of data output lanes (1 or 2), data frame width, and data rate. The data frame width is 20 or 24 bits and the data rate is SDR or DDR. 式 4 calculates the DCLK speed. 表 6-7 lists the possible values for the output data clock frequency.

$$\text{DCLK speed} = \frac{2 \text{ ADC channels } \times \text{ Data Frame Width (24 bit or 20 bit)}}{\text{Data Lanes (1 or 2)} \times \text{Data Rate(SDR} = 1, \text{ DDR} = 2)} \times \text{SMPL\_CLK} \quad (4)$$

ADVANCE INFORMATION

表 6-7. Data Clock (DCLK) Speed(1)

ADC CHANNELS	DATA FRAME WIDTH (Bits)	DATA RATE (1 = SDR, 2 = DDR)	OUTPUT LANES	SMPL_CLK MULTIPLIER	DCLK (SMPL_CLK = 5MHz)	DCLK (SMPL_CLK = 10MHz)	DCLK (SMPL_CLK = 20MHz)
2	24	1	1	48	240MHz	480MHz	—
			2	24	120MHz	240MHz	480MHz
		2	1	24	120MHz	240MHz	480MHz
			2	12	60MHz	120MHz	240MHz
	20	1	1	40	200MHz	400MHz	—
			2	20	100MHz	200MHz	400MHz
		2	1	20	100MHz	200MHz	400MHz
			2	10	50MHz	100MHz	200MHz

(1) The LVDS output data and clock are specified up to 600MHz. Faster speeds are not supported.

6.3.8.1 Data Frame Width

As shown in 図 6-6, the ADS921x supports 24-bit and 20-bit data frame width options. Configure the DATA_WIDTH field in address 0x12 to select the data frame width. The default output data frame width is 24 bits. The ADC resolution is 18 bits, represented by 20 bits. The two extra lower bits in the 20-bit data are ignored.

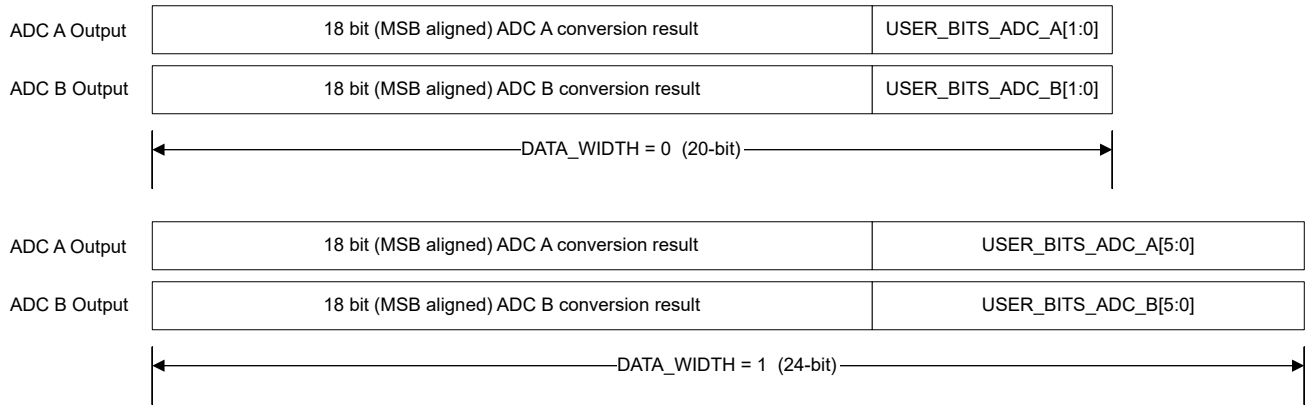


図 6-6. Data Frame Width Composition

6.3.8.2 Synchronizing Multiple ADCs

Drive the SMPL_CLK pins of the respective ADS921x devices with a common sampling clock. Match the timing delay on the clock path external to the ADCs by using identical PCB trace lengths for SMPL_CLK for the respective ADCs.

Use the SMPL_SYNC pin to synchronize multiple ADCs when using the internal decimation filter. The SMPL_SYNC pin is latched by the falling edge of the sampling clock. A pulse on SMPL_SYNC resets the internal decimation filter.

ADVANCE INFORMATION

6.3.8.3 Test Patterns for Data Interface

The ADS921x features test patterns (図 6-7) used by the host for debugging and verifying the data interface. The test patterns replace the ADC output data with predefined digital data. Enable the test patterns by configuring the corresponding register addresses 0x13 through 0x1B in bank 1.

表 6-8 lists the test patterns supported by the ADS921x.

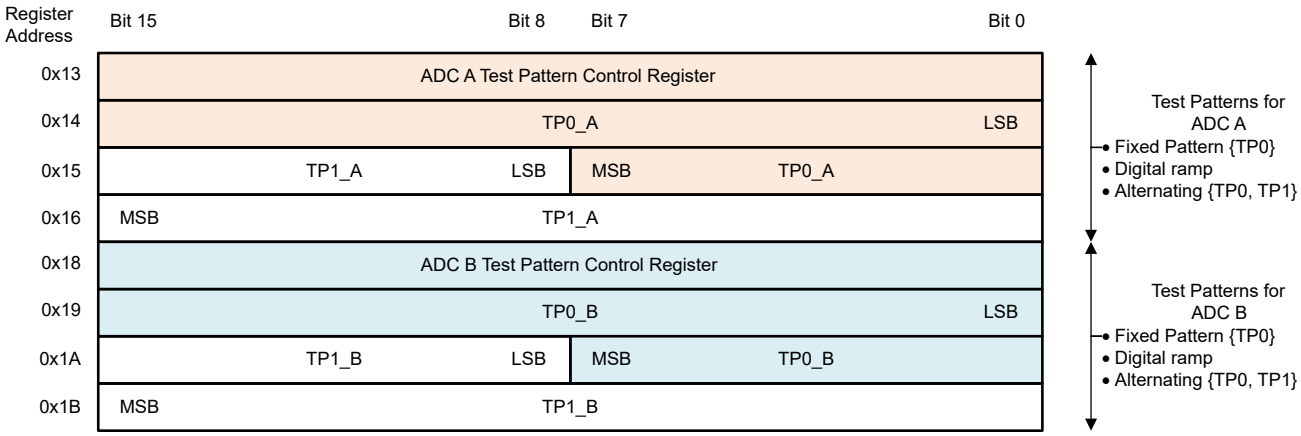


図 6-7. Register Bank for Test Patterns

表 6-8. Test Pattern Configurations

ADC OUTPUT	TP_EN_CHA TP_EN_CHB	TP_MODE_CHA TP_MODE_CHB	SECTION	RESULT#none#
ADC conversion result	0			
Fixed pattern	1	0 or 1	*Fixed Pattern*	ADC A = TP0_A ADC B = TP0_B
Digital ramp	1	2	*Digital Ramp*	ADC A = Digital ramp ADC B = Digital ramp
Alternating test patterns	1	3	*Alternating Test Pattern*	ADC A = TP0_A, TP1_A ADC B = TP0_B, TP1_B

注

1. Configure the test patterns for two separate channel groups ADC A and ADC B.

6.3.8.3.1 Fixed Pattern

The ADC outputs fixed patterns defined in the TP0_A and TP0_B registers in place of the ADC A and ADC B data, respectively.

- Configure the test patterns in TP0_A and TP0_B
- Set TP_EN_CHA = 1, TP_MODE_CHA = 0 (address = 0x13), TP_EN_CHB = 1, and TP_MODE_CHB = 0 (address = 0x18)

6.3.8.3.2 Alternating Test Pattern

The ADC outputs alternating test patterns defined in the TP0_A, TP1_A and TP0_B, TP1_B registers in place of the ADC A and ADC B data, respectively.

- Configure the test patterns in TP0_A, TP1_A, TP0_B, and TP1_B
- Set TP_EN_CHA = 1, TP_MODE_CHA = 3 (address = 0x13), TP_EN_CHB = 1, and TP_MODE_CHB = 3 (address = 0x18)

ADVANCE INFORMATION

6.3.8.3.3 Digital Ramp

The ADC outputs digital ramp values with increments specified in the RAMP_INC_A and RAMP_INC_B registers in place of the ADC A and ADC B data, respectively.

- Configure the increment value between two successive steps of the digital ramp in the RAMP_INC_A (address = 0x13) and RAMP_INC_B (address = 0x18) registers, respectively. The digital ramp increments by N + 1, where N is the value configured in these registers.
- Set TP_EN_CHA = 1, TP_MODE_CHA = 2 (address = 0x13), TP_EN_CHB = 1, and TP_MODE_CHB = 2 (address = 0x18)

6.3.9 ADC Sampling Clock Input

Use a low-jitter external clock with a high slew rate to maximize SNR performance. Operate the ADS921x with a differential or single-ended clock input. Clock amplitude impacts the ADC aperture jitter and consequently the SNR. For maximum SNR performance, provide a clock signal with fast slew rates that maximizes swing between IOVDD and GND levels.

The sampling clock must be a free-running continuous clock. The ADC generates a valid output data, data clock, and frame clock $t_{PU\_SMPL\_CLK}$, as specified in the *Switching Characteristics* after a free-running sampling clock is applied. The ADC output data, data clock, and frame clock are invalid when the sampling clock is stopped.

図 6-8 shows a diagram of the differential sampling clock input. For this configuration, connect the differential sampling clock input to the SMPL_CLKP and SMPL_CLKM pins. 図 6-9 shows a diagram of the single-ended sampling clock input. In this configuration, connect the single-ended sampling clock to SMPL_CLKP and connect SMPL_CLKM to ground.

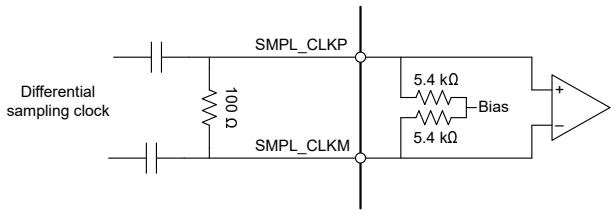


図 6-8. AC-Coupled Differential Sampling Clock

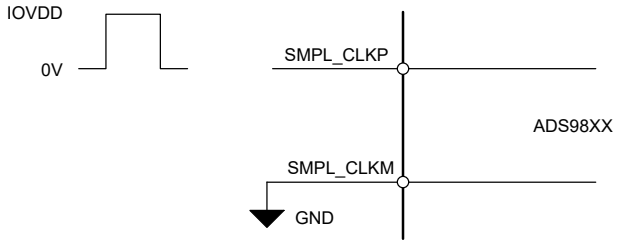


図 6-9. Single-Ended Sampling Clock

6.4 Device Functional Modes

6.4.1 Reset

Power down the ADS921x with a logic 0 on the $\overline{\text{RESET}}$ pin or by writing 1b to the RESET field (address 0x00, register bank 0). The device registers are initialized to the default values after reset. Initialize the device with a sequence of register write operations; see the *Initialization Sequence* section.

6.4.2 Power-Down Options

Power down the ADS921x with a logic 0 on the $\overline{\text{PWDN}}$ pin or by writing 11b to the PD_CH field (address 0xC0, register bank 1). The device registers are initialized to the default values after power-up. Initialize the device with a sequence of register write operations; see the *Initialization Sequence* section.

6.4.3 Normal Operation

In normal operating mode, the ADS921x is powered-up and digitizes the analog inputs at the falling edge of the sampling clock. The ADC outputs the data clock, frame clock, and MSB-aligned, 18 ビット conversion result.

ADVANCE INFORMATION

6.4.4 Initialization Sequence

As shown in 表 6-9, initialize the ADS921x with a sequence of register writes after device power-up or reset. Connect a free-running sampling clock to the ADC before executing the initialization sequence. The ADS921x registers are initialized with the default value after the initialization sequence is complete.

表 6-9. ADS921x Initialization Sequence

STEP NUMBER	REGISTER			COMMENT
	BANK	ADDRESS	VALUE[15:0]	
1	0	0x03	0x0002	Select register bank 1
2	1	0xF6	0x0002	INIT_2 = 1
3	0	0x04	0x000B	INIT_1 = 1011b
4	0	0x03	0x0010	Select register bank 2
5	2	0x12	0x0040	INIT_3 = 1
6	2	0x13	0x8000	INIT_4 = 1
7	2	0x0A	0x4000	INIT_5 = 1
8	Wait 10µs (min)			
9	2	0x0A	0x0000	INIT_5 = 0
10	0	0x03	0x0002	Select register bank 1
11	1	0xF6	0x0000	INIT_2 = 0
12	0	0x03	0x0010	Select register bank 2
13	2	0x13	0x0000	INIT_5 = 0
14	2	0x12	0x0000	INIT_4 = 0
15	0	0x04	0x0000	INIT_1 = 0
16	0	0x03	0x0002	Select register bank 1
17	1	0x33	0x0030	Write INIT_KEY
18	1	0xF4	0x0000	INIT = 0
19	1	0xF4	0x0002	INIT = 1
20	Wait 1ms (min)			
21	1	0xF4	0x0000	INIT = 0
22	Wait 1ms (min)			
23	1	0x33	0x0000	INIT_KEY = 0
24	1	0x0D	User defined	Enable gain error calibration and select ADC output data format
25	1	0x33	0x2040	Enable gain error calibration

ADVANCE INFORMATION

6.5 Programming

6.5.1 Register Write

Register write access is enabled by setting SPI_RD_EN = 0b. The 16-bit configuration registers are grouped in three register banks and are addressable with an 8-bit register address. Register bank 1 and register bank 2 are selected for read or write operation by configuring the PAGE_SEL0 and PAGE_SEL1 bits, respectively. Registers in bank 0 are always accessible, irrespective of the PAGE_SELx bits. The register addresses in bank 0 are unique and are not used in register banks 1 and 2.

As shown in 図 6-10, steps to write to a register are:

1. Frame 1: Write to register address 0x03 in register bank 0 to select either register bank 1 or bank 2 for a subsequent register write. This frame has no effect when writing to registers in bank 0.
2. Frame 2: Write to a register in the bank selected in frame 1. Repeat this step for writing to multiple registers in the same register bank.

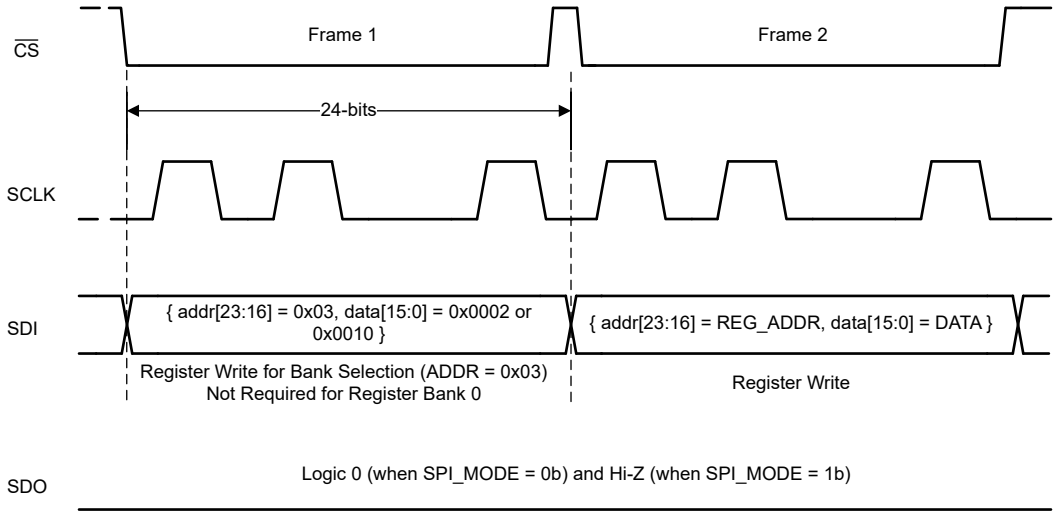


図 6-10. Register Write

6.5.2 Register Read

Select the desired register bank by writing to register address 0x03 in register bank 0. Register read access is enabled by setting SPI_RD_EN = 1b and SPI_MODE = 1b in register bank 0. As illustrated in 図 6-11, registers are read using two 24-bit SPI frames after SPI_RD_EN and SPI_MODE are set. The first SPI frame selects the register bank. The ADC returns the 16-bit register value in the second SPI frame corresponding to the 8-bit register address.

As illustrated in 図 6-11, steps to read a register are:

1. Frame 1: With SPI_RD_EN = 0b, write to register address 0x03 in register bank 0 to select the desired register bank 0 for reading.
2. Frame 2: Set SPI_RD_EN = 1b and SPI_MODE = 1b in register address 0x00 in register bank 0.
3. Frame 3: Read any register in the selected bank using a 24-bit SPI frame containing the desired register address. Repeat this step with the address of any register in the selected bank to read the corresponding register.
4. Frame 4: Set SPI_RD_EN = 0 to disable register reads and re-enable register writes.
5. Repeat steps 1 through 4 to read registers in a different bank.

ADVANCE INFORMATION

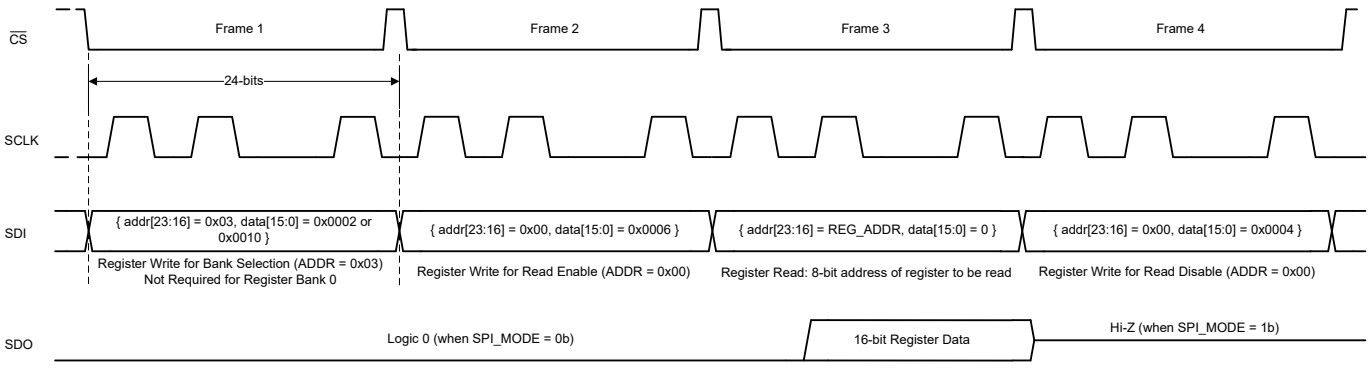


図 6-11. Register Read

6.5.3 Multiple Devices: Daisy-Chain Topology for SPI Configuration

図 6-12 shows a typical connection diagram showing multiple devices in a daisy-chain topology.

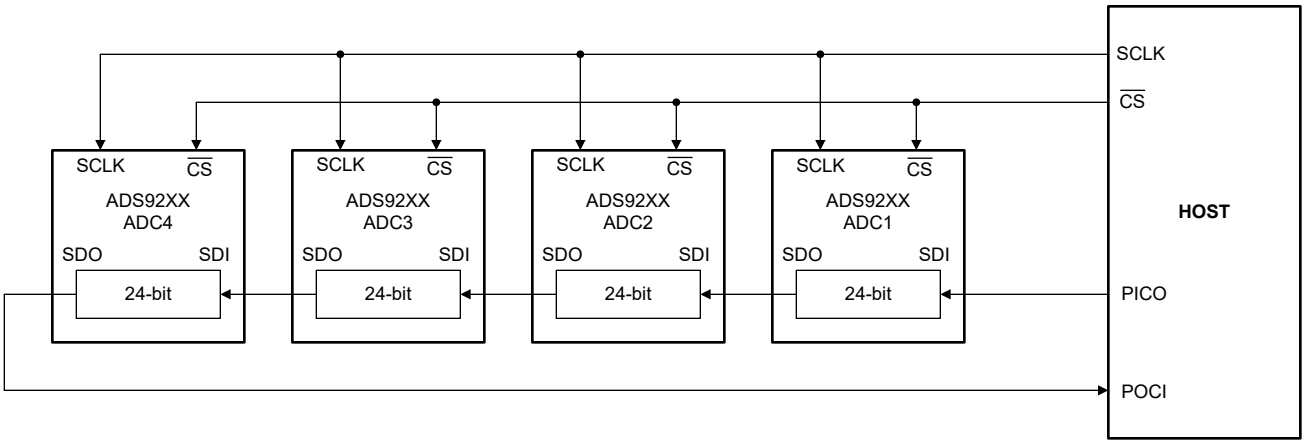


図 6-12. Daisy-Chain Connections for SPI Configuration

The $\overline{CS}$ and SCLK inputs of all ADCs are connected together and controlled by a single $\overline{CS}$ and SCLK pin of the controller, respectively. The SDI input pin of the first ADC in the chain (ADC1) is connected to the peripheral IN controller OUT (PICO) pin of the controller. The SDO output pin of ADC1 is connected to the SDI input pin of ADC2, and so on. The SDO output pin of the last ADC in the chain (ADC4) is connected to the peripheral OUT controller IN (POCI) pin of the controller. The data on the PICO pin passes through ADC1 with a 24-SCLK delay, as long as $\overline{CS}$ is active.

Enable daisy-chain mode after power-up or after the device is reset. Set the daisy-chain length in the DAISY_CHAIN_LENGTH register to enable daisy-chain mode. The daisy-chain length is the number of ADCs in the chain, excluding ADC1. In 図 6-12, the DAISY_CHAIN_LENGTH is 3.

6.5.3.1 Register Write With Daisy-Chain

Writing to registers in daisy-chain configuration requires N × 24 SCLKs in one SPI frame. Register writes in a daisy-chain configuration containing four ADCs, as illustrated in 図 6-12, requires 96 SCLKs.

The daisy-chain mode is enabled on power-up or after device reset. Configure the DAISY_CHAIN_LENGTH field to enable daisy-chain mode. Repeat the waveform in 図 6-13 N times, where N is the number of ADCs in the daisy chain. 図 6-14 provides the SPI waveform, containing N SPI frames, for enabling daisy-chain mode for N ADCs.

ADVANCE INFORMATION

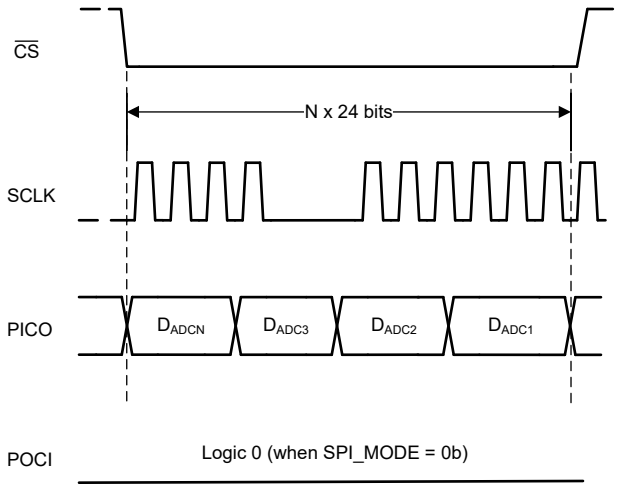


図 6-13. Register Write With Daisy-Chain

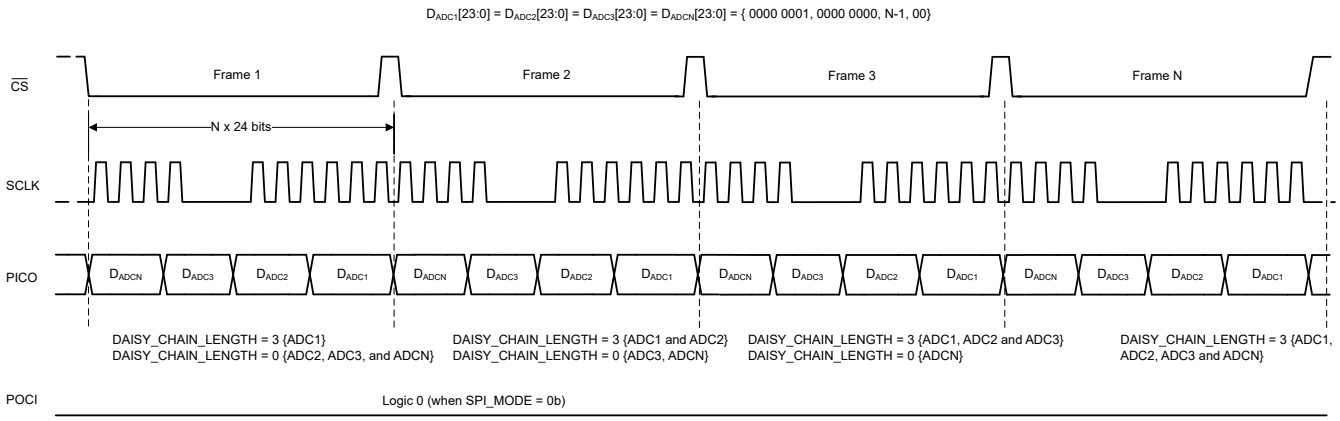


図 6-14. Register Write to Configure Daisy-Chain Length

6.5.3.2 Register Read With Daisy-Chain

図 6-15 illustrates an SPI waveform for reading registers in daisy-chain configuration. Steps for reading registers from N ADCs connected in daisy-chain are:

1. Register read is enabled by writing to the following registers:
   a. Write to PAGE_SEL to select the desired register bank
   b. Enable register reads by writing SPI_RD_EN = 0b (default on power-up)
2. With the register bank selected and SPI_RD_EN = 0b, the controller reads register data by:
   a. N × 24-bit SPI frame containing the 8-bit register address to be read: N times (0xFE, 0x00, 8-bit register address)
   b. N × 24-bit SPI frame to read out register data: N times (0xFF, 0xFF, 0xFF)

The 0xFE in step 2a configures the ADC for register read from the specified 8-bit address. At the end of step 2a, the output shift register in the ADC is loaded with register data. The ADC returns the 8-bit register address and corresponding 16-bit register data in step 2b.

ADVANCE INFORMATION

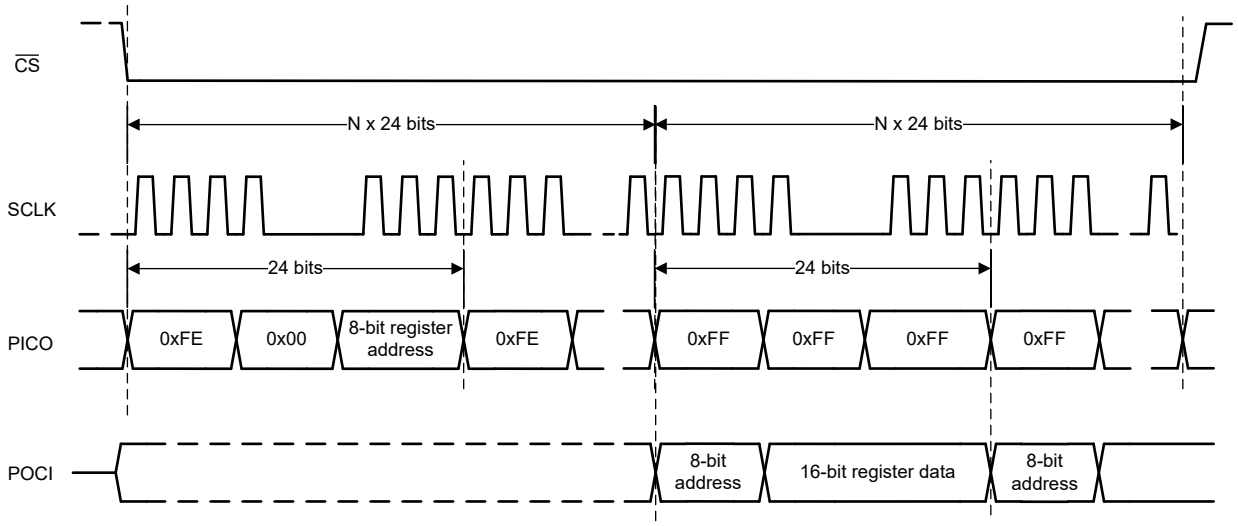


図 6-15. Register Read With Daisy-Chain Configuration

ADVANCE INFORMATION

7 Register Map

7.1 Register Bank 0

図 7-1. Register Bank 0 Map

ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00h	RESERVED													SPI_MODE	SPI_RD_EN	RESET
01h	RESERVED									DAISY_CHAIN_LEN					RESERVED	
03h	RESERVED									REG_BANK_SEL						
04h	RESERVED												INIT_1			
06h	REG_00H_READBACK															

表 7-1. Register Section/Block Access Type Codes

Access Type	Code	Description
R	R	Read
W	W	Write
R/W	R/W	Read or write
Reset or Default Value		
-n		Value after reset or the default value

7.1.2 Register 00h (offset = 0h) [reset = 0h]

図 7-2. Register 00h

15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED					SPI_MODE	SPI_RD_EN	RESET
W-0h					W-0h	W-0h	W-0h

図 7-3. Register 00h Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	W	0h	Reserved. Do not change from the default reset value.
2	SPI_MODE	W	0h	Select between legacy SPI mode and daisy-chain SPI mode for the configuration interface for register access. 0 : Daisy-chain SPI mode 1 : Legacy SPI mode
1	SPI_RD_EN	W	0h	Enable register read access in legacy SPI mode. This bit has no effect in daisy-chain SPI mode. 0 : Register read disabled 1 : Register read enabled
0	RESET	W	0h	ADC reset control. 0 : Normal device operation 1 : Reset ADC and all registers

ADVANCE INFORMATION

7.1.3 Register 01h (offset = 1h) [reset = 0h]

図 7-4. Register 01h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED	DAISY_CHAIN_LEN					RESERVED	
R/W-0h	R/W-0h					R/W-0h	

図 7-5. Register 01h Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
6-2	DAISY_CHAIN_LEN	R/W	0h	Configure the number of ADCs connected in daisy-chain for the SPI configuration. 0 : 1 ADC 1 : 2 ADCs 31 : 32 ADCs
1-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.1.4 Register 03h (offset = 3h) [reset = 2h]

図 7-6. Register 03h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
REG_BANK_SEL							
R/W-2h							

図 7-7. Register 03h Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
7-0	REG_BANK_SEL	R/W	2h	Register bank selection for read and write operations. 0 : Select register bank 0 2 : Select register bank 1 16 : Select register bank 2

ADVANCE INFORMATION

7.1.5 Register 04h (offset = 4h) [reset = 0h]

図 7-8. Register 04h

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				INIT_1			
R/W-0h							

図 7-9. Register 04h Field Descriptions

Bit	Field	Type	Reset	Description
3-0	INIT_1	R/W	0h	INIT_1 field for device initialization. Write 1011b during the initialization sequence. Write 0000b for normal operation.

7.1.6 Register 06h (offset = 6h) [reset = 2h]

図 7-10. Register 06h

15	14	13	12	11	10	9	8
REG_00H_READBACK							
R-0h							
7	6	5	4	3	2	1	0
REG_00H_READBACK							
R-5h							

図 7-11. Register 06h Field Descriptions

Bit	Field	Type	Reset	Description
15-0	REG_00H_READBACK	R	2h	This register is a copy of the register address 0x00 for readback. The register address 0x00 is write-only. The default readback value is 2h because SPI_RD_EN in address 0x00 must be set to 1 for register reads.

ADVANCE INFORMATION

7.2 Register Bank 1

図 7-12. Register Bank 1 Map

ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0Dh	RESERVED		DATA_FORMAT	RESERVED					GE_CAL_EN1	OSR_EN	OSR				RESERVED	
12h	RESERVED												XOR_EN	DATA_LANES		
13h	RESERVED								RAMP_INC_A				TP_MODE_CHA		TP_EN_CHA	RESERVED
14h	TP0_A															
15h	TP1_A								TP0_A							
16h	TP1_A															
18h	RESERVED								RAMP_INC_B				TP_MODE_CHB		TP_EN_CHB	RESERVED
19h	TP0_B															
1Ah	TP1_B								TP0_B							
1Bh	TP1_B															
1Ch	RESERVED		USER_BITS_ADC_B						RESERVED		USER_BITS_ADC_A					
33h	RESERVED		GE_CAL_EN3	RESERVED						GE_CAL_EN2	INIT_KEY		RESERVED			
90h	RESERVED	TS_LD	RESERVED													
91h	RESERVED						TEMPERATURE_SENSOR									
C0h	RESERVED		CLK1	OSR_INIT1			OSR_CLK			RESERVED					PD_CH	
C1h	RESERVED			PD_REF	RESERVED		DATA_RATE		RESERVED							CLK2
C4h	RESERVED										OSR_INIT2		RESERVED		OSR_INIT3	PD_CHIP
C5h	RESERVED						CLK3		RESERVED							
F4h	RESERVED														INIT	RESERVED
F6h	RESERVED														INIT_2	RESERVED
FBh	RESERVED												NCO_SYSREF	XOR_MODE	RESERVED	MIXER_EN
FCh	NCO_PHASE_COUNT[15:0]															
FDh	NCO_FREQUENCY[7:0]								NCO_PHASE_COUNT[23:16]							
FEh	NCO_FREQUENCY[23:8]															

表 7-2. Register Section/Block Access Type Codes

Access Type	Code	Description
R	R	Read
W	W	Write
R/W	R/W	Read or write
Reset or Default Value		
-n		Value after reset or the default value

ADVANCE INFORMATION

7.2.1 Register 0Dh (offset = Dh) [reset = 2002h]

図 7-13. Register 0Dh

15	14	13	12	11	10	9	8
RESERVED		DATA_FORMAT	RESERVED				
R/W-0h		R/W-1h	R/W-0h				
7	6	5	4	3	2	1	0
GE_CAL_EN1	OSR_EN	OSR				RESERVED	
R/W-0h	R/W-2h						

図 7-14. Register 0Dh Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
13	DATA_FORMAT	R/W	1h	Select data format for the ADC conversion result. 0 : Straight binary format 1 : Two's-complement format
12-8	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
7-7	GE_CAL_EN1	R/W	0h	Global control for gain error calibration. 0 : Gain error calibration disabled for all channels 1 : Gain error calibration enabled for all channels
6-6	OSR_EN	R/W	0h	Control for data averaging depth. 0 : Data averaging disabled 1 : Data averaging enabled
5-2	OSR	R/W	0h	Control for enabling data averaging. 0 : 2 samples averaged 1 : 4 samples averaged 2 : 8 samples averaged 3 : 16 samples averaged
1-0	RESERVED	R/W	2h	Reserved. Do not change from the default reset value.

ADVANCE INFORMATION

7.2.2 Register 12h (offset = 12h) [reset = 2h]

図 7-15. Register 12h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				XOR_EN	DATA_LANES		
R/W-0h				R/W-0h	R/W-2h		

図 7-16. Register 12h Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
3	XOR_EN	R/W	0h	Enables XOR operation on ADC conversion result. 0 : XOR operation is disabled 1 : ADC conversion result is bit-wise XOR with the LSB of the ADC conversion result
2-0	DATA_LANES	R/W	2h	Selects the number of output data lanes and number of data bits per output lane. Enables XOR operation on ADC conversion result. 0 : ADC A and B data output on DOUTA and DOUTB respectively; 20 bits per ADC. 2 : ADC A and B data output on DOUTA and DOUTB respectively; 24 bits per ADC. 5 : ADC A and B data output on DOUTA; 20 bits per ADC. 7 : ADC A and B data output on DOUTA; 24 bits per ADC.

ADVANCE INFORMATION

7.2.3 Register 13h (offset = 13h) [reset = 0h]

図 7-17. Register 13h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RAMP_INC_A				TP_MODE_A		TP_EN_A	RESERVED
R/W-0h				R/W-0h		R/W-0h	R/W-0h

図 7-18. Register 13h Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
7-4	RAMP_INC_A	R/W	0h	Increment value for the ramp pattern output. The output ramp increments by N+1, where N is the value configured in this register.
3-2	TP_MODE_A	R/W	0h	Select digital test pattern for ADC A. 0 : Fixed pattern from the TP0_A register 1 : Fixed pattern from the TP0_A register 2 : Digital ramp output 3 : Alternate fixed pattern output from the TP0_A and TP1_A registers
1	TP_EN_A	R/W	0h	Enable digital test pattern for data corresponding to ADC A. 0 : Data output is the ADC conversion result 1 : Data output is the digital test pattern for ACD A
0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.2.4 Register 14h (offset = 14h) [reset = 0h]

図 7-19. Register 14h

15	14	13	12	11	10	9	8
TP0_A[15:0]							
R/W-0h							
7	6	5	4	3	2	1	0
TP0_A[15:0]							
R/W-0h							

図 7-20. Register 14h Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TP0_A[15:0]	R/W	0h	Lower 16 bits of test pattern 0

ADVANCE INFORMATION

7.2.5 Register 15h (offset = 15h) [reset = 0h]

図 7-21. Register 15h

15	14	13	12	11	10	9	8
TP1_A[7:0]							
R/W-0h							
7	6	5	4	3	2	1	0
TP0_A[23:16]							
R/W-0h							

図 7-22. Register 15h Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TP1_A[7:0]	R/W	0h	Lower eight bits of test pattern 1
7-0	TP0_A[23:16]	R/W	0h	Upper eight bits of test pattern 0

7.2.6 Register 16h (offset = 16h) [reset = 0h]

図 7-23. Register 16h

15	14	13	12	11	10	9	8
TP1_A[23:8]							
R/W-0h							
7	6	5	4	3	2	1	0
TP1_A[23:8]							
R/W-0h							

図 7-24. Register 16h Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TP1_A[23:8]	R/W	0h	Upper 16 bits of test pattern 1

ADVANCE INFORMATION

7.2.7 Register 18h (offset = 18h) [reset = 0h]

図 7-25. Register 18h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RAMP_INC_B				TP_MODE_B		TP_EN_B	RESERVED
R/W-0h				R/W-0h		R/W-0h	R/W-0h

図 7-26. Register 18h Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
7-4	RAMP_INC_B	R/W	0h	Increment value for the ramp pattern output. The output ramp increments by N+1, where N is the value configured in this register.
3-2	TP_MODE_B	R/W	0h	Select digital test pattern for ADC B. 0 : Fixed pattern from the TP0_B register 1 : Fixed pattern from the TP0_B register 2 : Digital ramp output 3 : Alternate fixed pattern output from the TP0_B and TP1_B registers
1	TP_EN_B	R/W	0h	Enable digital test pattern for data corresponding to ADC B. 0 : Data output is the ADC conversion result 1 : Data output is the digital test pattern
0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.2.8 Register 19h (offset = 19h) [reset = 0h]

図 7-27. Register 19h

15	14	13	12	11	10	9	8
TP0_B[15:0]							
R/W-0h							
7	6	5	4	3	2	1	0
TP0_B[15:0]							
R/W-0h							

図 7-28. Register 19h Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TP0_B[15:0]	R/W	0h	Lower 16 bits of test pattern 0

ADVANCE INFORMATION

7.2.9 Register 1Ah (offset = 1Ah) [reset = 0h]

図 7-29. Register 1Ah

15	14	13	12	11	10	9	8
TP1_B[7:0]							
R/W-0h							
7	6	5	4	3	2	1	0
TP0_B[23:16]							
R/W-0h							

図 7-30. Register 1Ah Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TP1_B[7:0]	R/W	0h	Lower eight bits of test pattern 1
7-0	TP0_B[23:16]	R/W	0h	Upper eight bits of test pattern 0

7.2.10 Register 1Ch (offset = 1Ch) [reset = 0h]

図 7-31. Register 1Ch

15	14	13	12	11	10	9	8
RESERVED		USER_BITS_ADC_B					
R/W-0h		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED		USER_BITS_ADC_A					
R/W-0h		R/W-0h					

図 7-32. Register 1Ch Field Descriptions

Bit	Field	Type	Reset	Description
15-8	USER_BITS_ADC_B	R/W	0h	User-defined bits appended to the ADC conversion result from ADC B.
7-0	USER_BITS_ADC_A	R/W	0h	User-defined bits appended to the ADC conversion result from ADC A.

7.2.11 Register 33h (offset = 33h) [reset = 0h]

図 7-33. Register 33h

15	14	13	12	11	10	9	8
RESERVED		GE_CAL_EN3	RESERVED				
R/W-0h		R/W-0h	R/W-0h				
7	6	5	4	3	2	1	0
RESERVED	GE_CAL_EN2	INIT_KEY		RESERVED			
R/W-0h	R/W-0h	R/W-0h		R/W-0h			

図 7-34. Register 33h Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
13	GE_CAL_EN3	R/W	0h	Global control for gain error calibration. 0 : Gain error calibration disabled for all channels 1 : Gain error calibration enabled for all channels
12-7	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
6	GE_CAL_EN2	R/W	0h	Global control for gain error calibration. 0 : Gain error calibration disabled for all channels 1 : Gain error calibration enabled for all channels
5-4	INIT_KEY	R/W	0h	Device initialization sequence access key. Write 11b to access the device initialization sequence. Write 00b for normal operation.
3-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

ADVANCE INFORMATION

7.2.12 Register 90h (offset = 90h) [reset = 0h]

図 7-35. Register 90h

15	14	13	12	11	10	9	8
RESERVED	TS_LD	RESERVED					
R/W-0h	R/W-0h	R/W-0h					
7	6	5	4	3	2	1	0
RESERVED							
R/W-0h							

図 7-36. Register 90h Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
14	TS_LD	R/W	0h	Trigger to load temperature sensor output in address 0x91. Transition from 0 to 1 if this bit triggers the data load operation.
13-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

ADVANCE INFORMATION

7.2.13 Register 91h (offset = 91h) [reset = 00h]

図 7-37. Register 91h

15	14	13	12	11	10	9	8
RESERVED						TEMPERATURE_SENSOR	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
TEMPERATURE_SENSOR							
R/W-0h							

図 7-38. Register 91h Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
9-0	TEMPERATURE_SENSOR	R/W	0h	10-bit temperature sensor output. See the *Temperature Sensor* section.

7.2.14 Register C0h (offset = C0h) [reset = 0h]

図 7-39. Register C0h

15	14	13	12	11	10	9	8
RESERVED			CLK1	OSR_INIT1		OSR_CLK	
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OSR_CLK	RESERVED					PD_CH	
R/W-0h	R/W-0h					R/W-0h	

図 7-40. Register C0h Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
12-12	CLK1	R/W	0h	Selects the clock configuration based on output data-lanes. 0 : Configuration for DATA_LANES = 0 or 2 1 : Configuration for DATA_LANES = 5 or 7
11-10	OSR_INIT1	R/W	0h	Initialization for data averaging. 0 : Configuration for disabling data averaging 1 : Configuration for enabling data averaging
9-7	OSR_CLK	R/W	0h	Data output clock configuration for data averaging. See 表 6-3 for more details.
6-2	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
1-0	PD_CH	R/W	0h	Power-down control for the analog input channels. 0 : Normal operation 1 : ADC A powered down 2 : ADC B powered down 3 : ADC A and B powered down

ADVANCE INFORMATION

7.2.15 Register C1h (offset = C1h) [reset = 0h]

図 7-41. Register C1h

15	14	13	12	11	10	9	8
RESERVED				PD_REF	RESERVED		DATA_RATE
R/W-0h				R/W-0h	R/W-0h		R/W-0h
7	6	5	4	3	2	1	0
RESERVED							CLK2
R/W-0h							R/W-0h

図 7-42. Register C1h Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
11	PD_REF	R/W	0h	ADC reference voltage source selection. 0 : Internal reference enabled. 1 : Internal reference disabled. Connect the external reference voltage to the REFIO pin.
10-9	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
8	DATA_RATE	R/W	0h	Select data rate for the data interface. 0 : Double data rate (DDR) 1 : Single data rate (SDR)
7-1	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
0	CLK2	R/W	0h	Select data rate for the data interface. 0 : Configuration for DATA_LANES = 2 or 7 1 : Configuration for DATA_LANES = 0 or 5

ADVANCE INFORMATION

7.2.16 Register C4h (offset = C4h) [reset = 0h]

図 7-43. Register C4h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		OSR_INIT2		RESERVED		OSR_INIT3	PD_CHIP
R/W-0h		R/W-0h		R/W-0h		R/W-0h	R/W-0h

図 7-44. Register C4h Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
5-4	OSR_INIT2	R/W	0h	Initialization for data averaging. 0 : Configuration for disabling data averaging 2 : Configuration for enabling data averaging
3-2	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
1-1	OSR_INIT3	R/W	0h	Initialization for data averaging. 0 : Configuration for disabling data averaging 1 : Configuration for enabling data averaging
0-0	PD_CHIP	R/W	0h	Full chip power-down control. 0 : Normal device operation 1 : Full device powered-down

ADVANCE INFORMATION

7.2.17 Register C5h (offset = C5h) [reset = 0h]

図 7-45. Register C5h

15	14	13	12	11	10	9	8
RESERVED						CLK3	RESERVED
R/W-0h						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED							
R/W-0h							

図 7-46. Register C5h Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
9	CLK3	R/W	0h	Select data rate for the data interface. 0 : Configuration for DATA_LANES = 0 or 2 1 : Configuration for DATA_LANES = 5 or 7

7.2.18 Register F4h (offset = F4h) [reset = 0h]

図 7-47. Register F4h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						CM_CTRL_EN	RESERVED
R/W-0h						R/W-0h	R/W-0h

図 7-48. Register F4h Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
1	INIT	R/W	0h	INIT field for device initialization. Write 1b during the initialization sequence. Write 0b for normal operation.
0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

ADVANCE INFORMATION

7.2.19 Register F6h (offset = F6h) [reset = 0h]

図 7-49. Register F6h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						INIT_2	RESERVED
R/W-0h						R/W-0h	R/W-0h

図 7-50. Register F6h Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
1	INIT_2	R/W	0h	INIT_2 field for device initialization. Write 1b during the initialization sequence. Write 0b for normal operation.
0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

ADVANCE INFORMATION

7.2.20 Register FBh (offset = FBh) [reset = 0h]

図 7-51. Register FBh

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				NCO_SYSREF	XOR_MODE	RESERVED	MIXER_EN
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

図 7-52. Register FBh Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
3	NCO_SYSREF	R/W	0h	Set to 1b when applying periodic pulses on the SMPL_SYNC pin. 0: Synchronize the NCO with one pulse on the SMPL_SYNC pin. 1: Synchronize the NCO with the first pulse on the SMPL_SYNC pin when using periodic pulses.
2	XOR_MODE	R/W	0h	Selects the bit with which the ADC output data is XOR'ed when XOR output mode is enabled. 0 : PRBS bit is output after the ADC LSB. ADC output data is XOR'ed with the PRBS bit. 1 : ADC output data is XOR'ed with the LSB of the conversion result.
1	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
0	MIXER_EN	R/W	0h	0: Digital down converter disabled 1: Digital down converter enabled

ADVANCE INFORMATION

7.2.21 Register FCh (offset = FCh) [reset = 0h]

図 7-53. Register FCh

15	14	13	12	11	10	9	8
NCO_PHASE_COUNT							
R/W-0h							
7	6	5	4	3	2	1	0
NCO_PHASE_COUNT							
R/W-0h							

図 7-54. Register FCh Field Descriptions

Bit	Field	Type	Reset	Description
15-0	NCO_PHASE_COUNT[15:0]	R/W	0h	Lower 15 bits of the NCO phase count. See the *Digital Down Converter* section.

ADVANCE INFORMATION

7.2.22 Register FDh (offset = FDh) [reset = 0h]

図 7-55. Register FDh

15	14	13	12	11	10	9	8
NCO_FREQUENCY							
R/W-0h							
7	6	5	4	3	2	1	0
NCO_PHASE_COUNT							
R/W-0h							

図 7-56. Register FDh Field Descriptions

Bit	Field	Type	Reset	Description
15-8	NCO_FREQUENCY[7:0]	R/W	0h	Lower eight bits of the NCO phase count. See the *Digital Down Converter* section.
7-0	NCO_PHASE_COUNT[23:16]	R/W	0h	Higher eight bits of the NCO phase count. See the *Digital Down Converter* section.

ADVANCE INFORMATION

7.2.23 Register FEh (offset = FEh) [reset = 0h]

図 7-57. Register FEh

15	14	13	12	11	10	9	8
NCO_FREQUENCY							
R/W-0h							
7	6	5	4	3	2	1	0
NCO_FREQUENCY							
R/W-0h							

図 7-58. Register FEh Field Descriptions

Bit	Field	Type	Reset	Description
15-0	NCO_FREQUENCY	R/W	0h	Higher 16 bits of the NCO phase count. See the *Digital Down Converter* section.

ADVANCE INFORMATION

7.3 Register Bank 2

図 7-59. Register Bank 2 Map

ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
12h	RESERVED									INIT_3	RESERVED					
13h	INIT_4	RESERVED														
0Ah	RESERVED	INIT_2	RESERVED													

表 7-3. Register Section/Block Access Type Codes

Access Type	Code	Description
R	R	Read
W	W	Write
R/W	R/W	Read or write
Reset or Default Value		
-n		Value after reset or the default value

7.3.1 Register 12h (offset = 12h) [reset = 0h]

図 7-60. Register 12h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED	INIT_3	RESERVED					
R/W-0h	R/W-0h	R/W-0h					

図 7-61. Register 12 Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
6-6	INIT_3	R/W	0h	INIT_3 field for device initialization. Write 1b during the initialization sequence. Write 0b for normal operation.
5-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.3.2 Register 13h (offset = 13h) [reset = 0h]

図 7-62. Register 13h

15	14	13	12	11	10	9	8
INIT_4	RESERVED						
R/W-0h	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED							
R/W-0h							

図 7-63. Register 13 Field Descriptions

Bit	Field	Type	Reset	Description
15-15	INIT_4	R/W	0h	INIT_4 field for device initialization. Write 1b during initialization sequence. Write 0b for normal operation.

ADVANCE INFORMATION

図 7-63. Register 13 Field Descriptions (続き)

Bit	Field	Type	Reset	Description
14-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.3.3 Register 0Ah (offset = 0Ah) [reset = 0h]

図 7-64. Register 0Ah

15	14	13	12	11	10	9	8
RESERVED	INIT_5	RESERVED					
R/W-0h	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED							
R/W-0h							

図 7-65. Register 0A Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
14	INIT_5	R/W	0h	INIT_5 field for device initialization. Write 1b during initialization sequence. Write 0b for normal operation.
13-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

ADVANCE INFORMATION

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ADS921x features an integrated ADC driver, low-latency, high-speed, low AC and DC errors, and low temperature drift. These features make the ADS921x a high-performance signal-chain for applications where precision measurements with low-latency are required. The following section gives an example circuit and recommendations for using the ADS921x device family in a data acquisition (DAQ) system.

8.2 Typical Applications

8.2.1 Data Acquisition (DAQ) Circuit for ≤20kHz Input Signal Bandwidth

図 8-1 shows a 2-channel signal-chain with minimum external components. This signal-chain significantly reduces solution size by driving the ADS921x with the 2-channel, fully differential amplifier (FDA) THS4552.

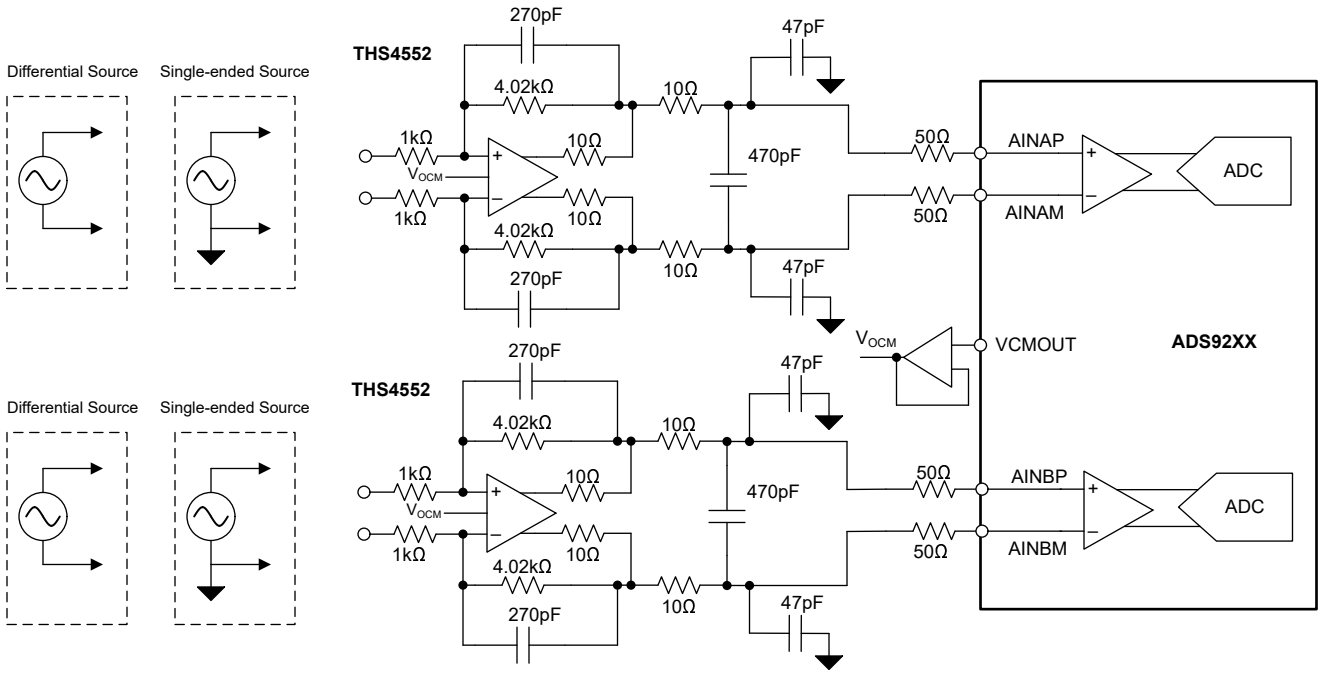


図 8-1. Data Acquisition (DAQ) Circuit for ≤20kHz Input Signal Bandwidth

8.2.1.1 Design Requirements

表 8-1 lists the parameters for this typical application.

表 8-1. Design Parameters

PARAMETER	VALUE
SNR	≥ 92dB
THD	≤ –110dB
Input signal frequency	≤ 20kHz

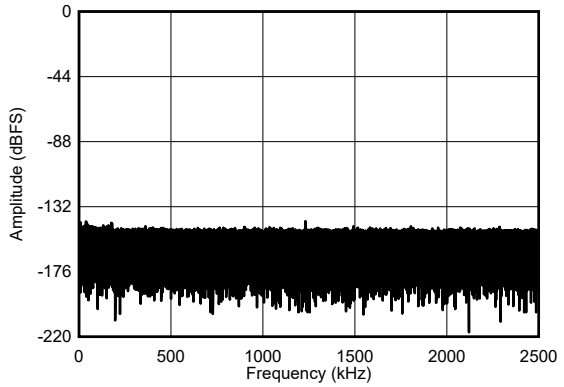
8.2.1.2 Detailed Design Procedure

Use the procedure discussed in this section for any ADS921x application circuit.

- All ADS921x applications require the supply decoupling as provided in the *Power Supply Recommendations* section.
- Make sure the values provided in this section meet the maximum throughput and input signal frequency design requirements given. Use a lower bandwidth signal chain when lower noise performance is required.

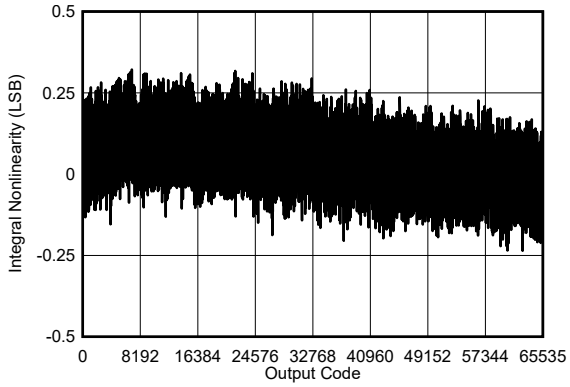
8.2.1.3 Application Curves

図 8-2 and 図 8-3 show the SNR and INL performance for the circuit in 図 8-1, respectively.



f_{IN} = 2kHz, SNR = 93.4dBFS, THD = –120dB

図 8-2. Typical FFT at 5MSPS/Channel: ADS9217



f_{IN} = 2kHz, INL = ±0.3LSB

図 8-3. Typical INL at 5MSPS/Channel: ADS9217

ADVANCE INFORMATION

8.2.2 Data Acquisition (DAQ) Circuit for ≤100kHz Input Signal Bandwidth

図 8-4 shows a 2-channel signal-chain with minimum external components. This signal-chain significantly reduces solution size by driving the ADS921x with the 2-channel, fully differential amplifier (FDA) THS4552.

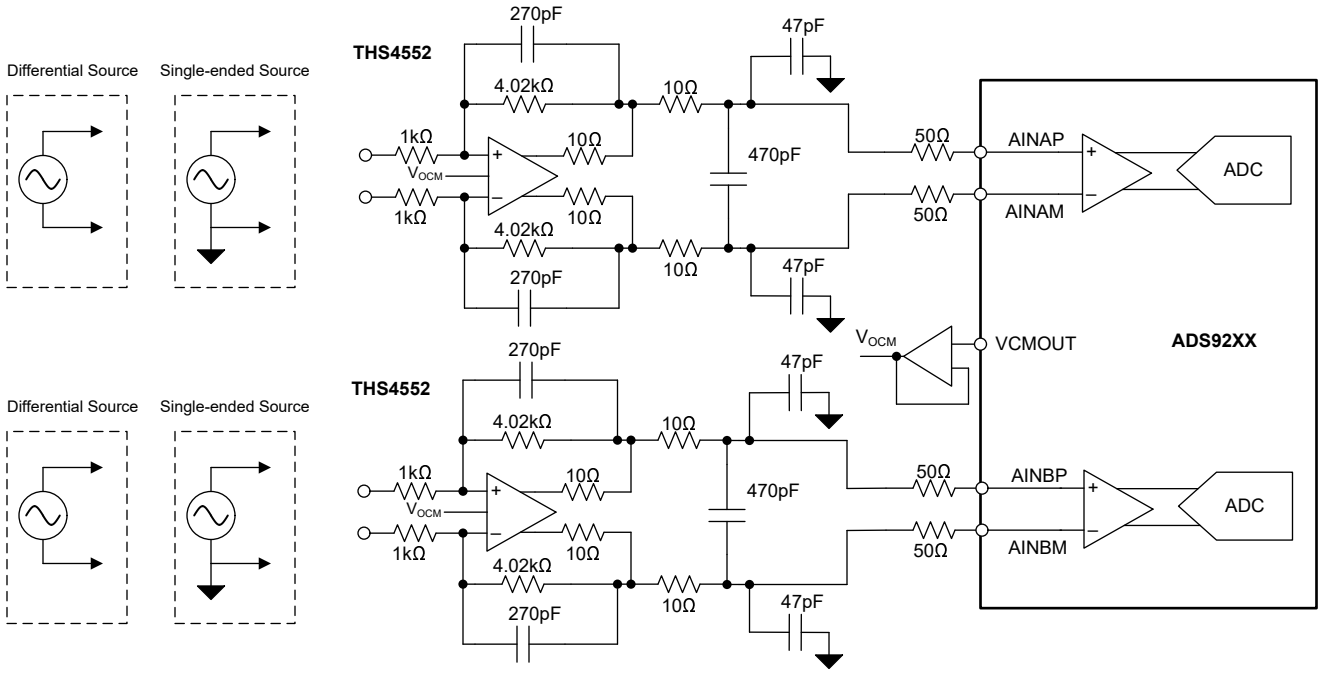


図 8-4. Data Acquisition (DAQ) Circuit for ≤100kHz Input Signal Bandwidth

8.2.2.1 Design Requirements

表 8-2 lists the parameters for this typical application.

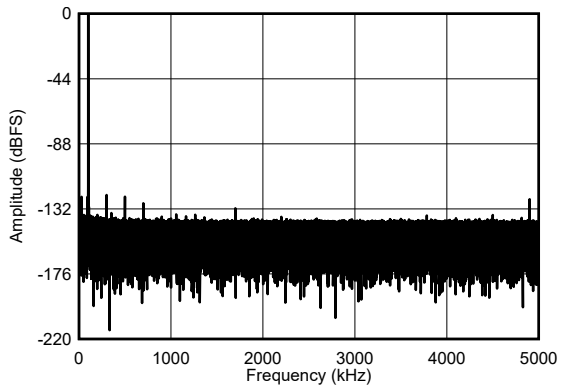
表 8-2. Design Parameters

PARAMETER	VALUE
SNR	≥ 91dB
THD	≤ –110dB
Input signal frequency	≤ 100kHz

ADVANCE INFORMATION

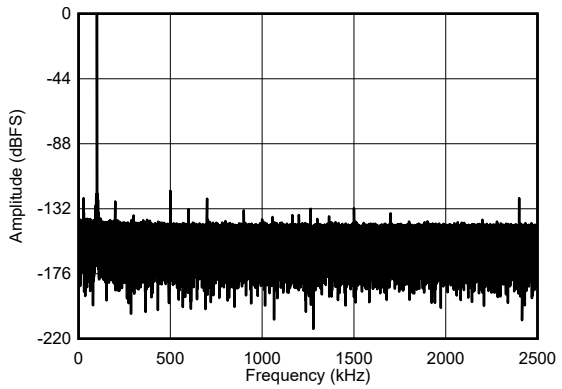
8.2.2.2 Application Curves

図 8-5 and 図 8-6 show the FFT plots for the circuit in 図 8-4.



f_{IN} = 100kHz, SNR = 92dB, THD = –117dB

図 8-5. Typical FFT at 10MSPS/Channel: ADS9218



f_{IN} = 100kHz, SNR = 92dB, THD = –117dB

図 8-6. Typical FFT at 5MSPS/Channel: ADS9217

8.2.3 Data Acquisition (DAQ) Circuit for ≤1MHz Input Signal Bandwidth

図 8-7 shows a 2-channel solution with minimum external components. This signal-chain significantly reduces signal-chain size by driving the ADS9219 with the THS4541, which enables low-distortion performance with low power over wide signal bandwidth.

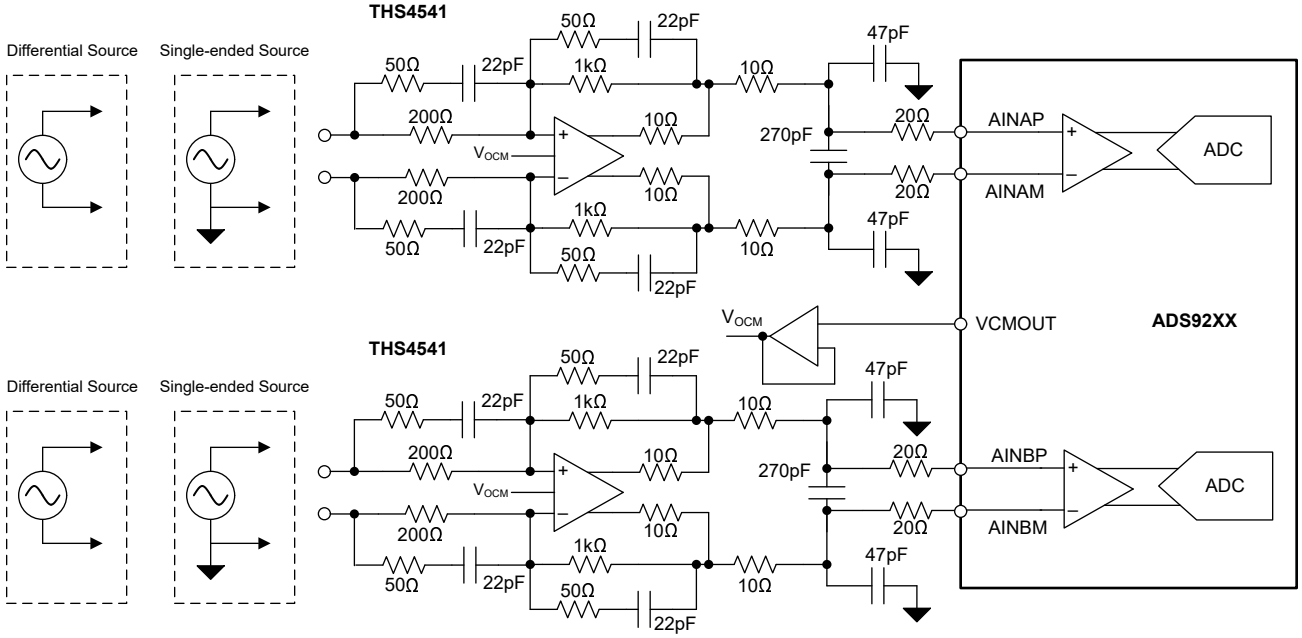


図 8-7. Data Acquisition (DAQ) Circuit for ≤1MHz Input Signal Bandwidth

ADVANCE INFORMATION

8.2.3.1 Design Requirements

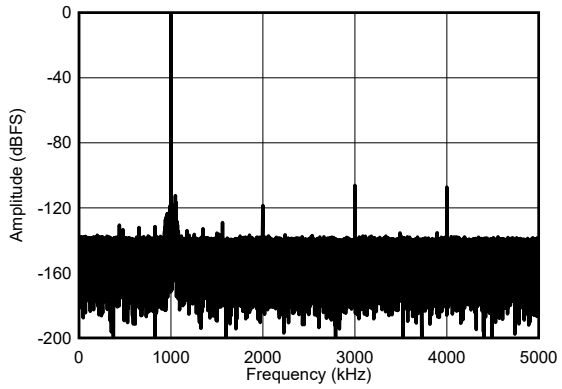
表 8-3 lists the parameters for this typical application.

表 8-3. Design Parameters

PARAMETER	VALUE
SNR	≥ 80dB
THD	≤ –100dB
Input signal frequency	≤ 1MHz

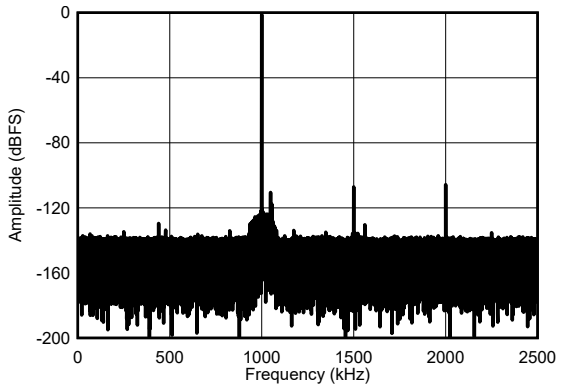
8.2.3.2 Application Curves

図 8-8 and 図 8-9 show the FFT plots for the circuit in 図 8-7.



f_{IN} = 1MHz, SNR = 90.6dB, THD = –104dB

図 8-8. Typical FFT at 10MSPS/Channel: ADS9218



f_{IN} = 1MHz, SNR = 90.5dB, THD = –104.2dB

図 8-9. Typical FFT at 5MSPS/Channel: ADS9217

ADVANCE INFORMATION

8.3 Power Supply Recommendations

The ADS921x has three independent power supplies, AVDD_5V, AVDD_1V8, and DVDD_1V8. The AVDD_5V supply provides power to the ADC driver. The AVDD_1V8 provides power to the analog circuits. The DVDD_1V8 supply provides power to the digital interface. Set the AVDD_5, AVDD_1V8, and DVDD_1V8 supplies independently to voltages within the permissible range. 図 8-10 shows how to decouple the power supplies.

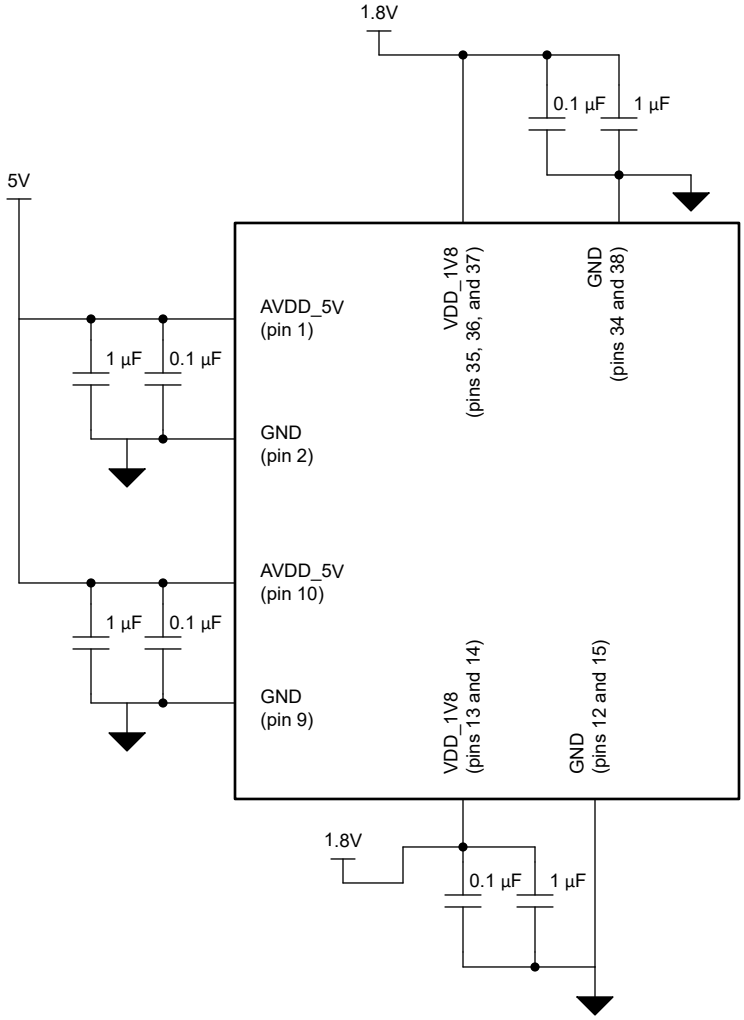


図 8-10. Power-Supply Decoupling

ADVANCE INFORMATION

8.4 Layout

8.4.1 Layout Guidelines

図 8-11 shows a board layout example for the ADS921x. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference signals away from noise sources. Use 0.1µF ceramic bypass capacitors in close proximity to the analog (AVDD_5V and VDD_1V8), and digital (VDD_1V8) power-supply pins. Avoid placing vias between the power-supply pins and the bypass capacitors. Place the reference decoupling capacitor close to the device REFIO and REFM pins. Avoid placing vias between the REFIO pin and the bypass capacitors. Connect the GND and REFM pins to a ground plane using short, low-impedance paths.

8.4.2 Layout Example

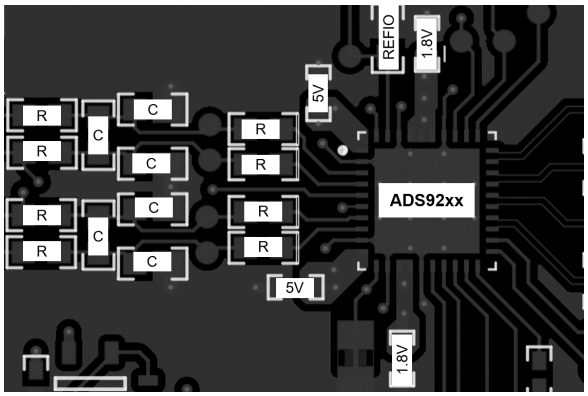


図 8-11. Example Layout

ADVANCE INFORMATION

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *REF70 2 ppm/°C Maximum Drift, 0.23 ppm$_{p-p}$ 1/f Noise, Precision Voltage Reference*, data sheet
- Texas Instruments, *THS4552 Dual-Channel, Low-Noise, Precision, 150-MHz, Fully Differential Amplifier*, data sheet
- Texas Instruments, *THS4541 Negative Rail Input, Rail-to-Rail Output, Precision, 850-MHz Fully Differential Amplifier*, data sheet

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

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9.4 Trademarks

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9.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (January 2023) to Revision A (April 2024)	Page
• 「事前情報」デバイスとして ADS9219 をドキュメントに追加	1

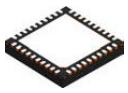
ADVANCE INFORMATION

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

11.1 Mechanical Data

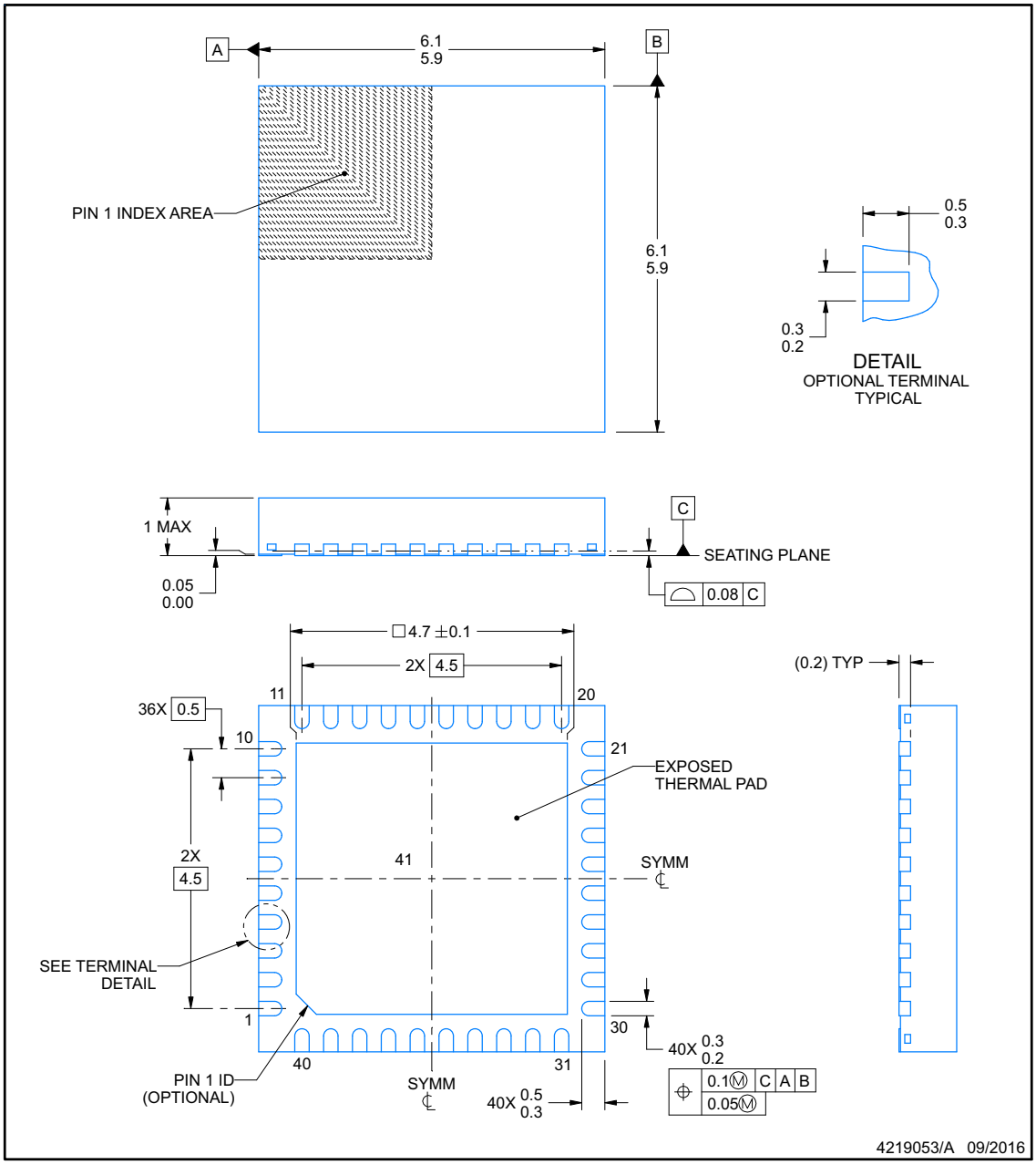


RHA0040C

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

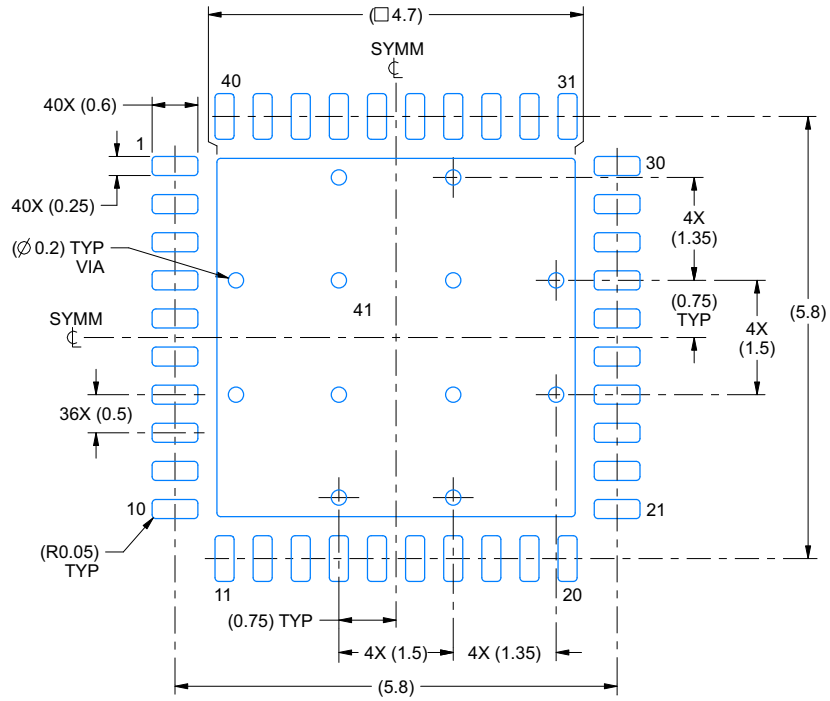
ADVANCE INFORMATION

ADVANCE INFORMATION

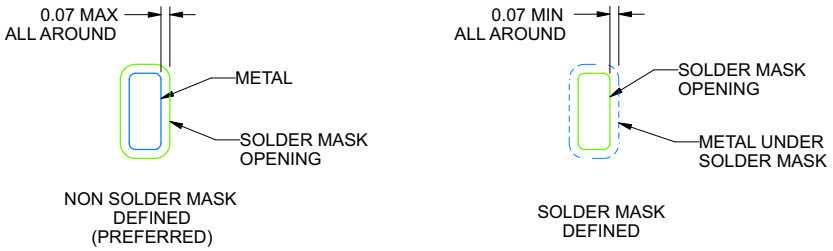
EXAMPLE BOARD LAYOUT

RHA0040C — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:12X



SOLDER MASK DETAILS

4219053/A 09/2016

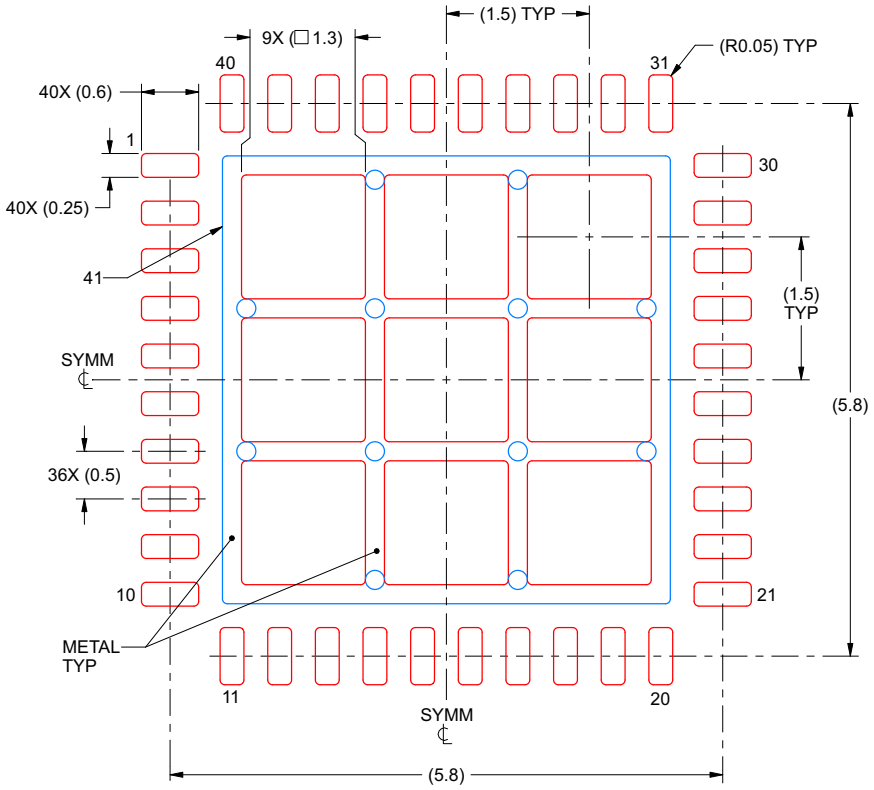
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHA0040C **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
69% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

4219053/A 09/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

重要なお知らせと免責事項

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PADS9218RHAT	ACTIVE	VQFN	RHA	40	250	TBD	Call TI	Call TI	-40 to 125		Samples
PADS9219RHAR	ACTIVE	VQFN	RHA	40	4000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

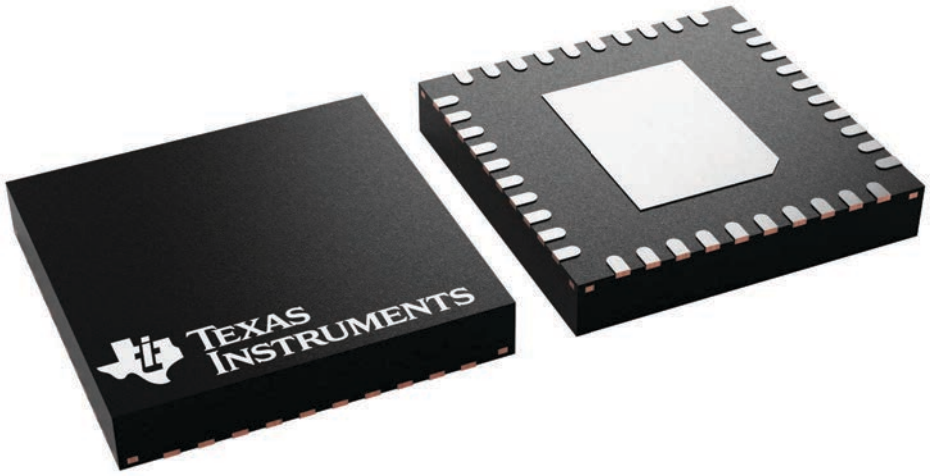
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



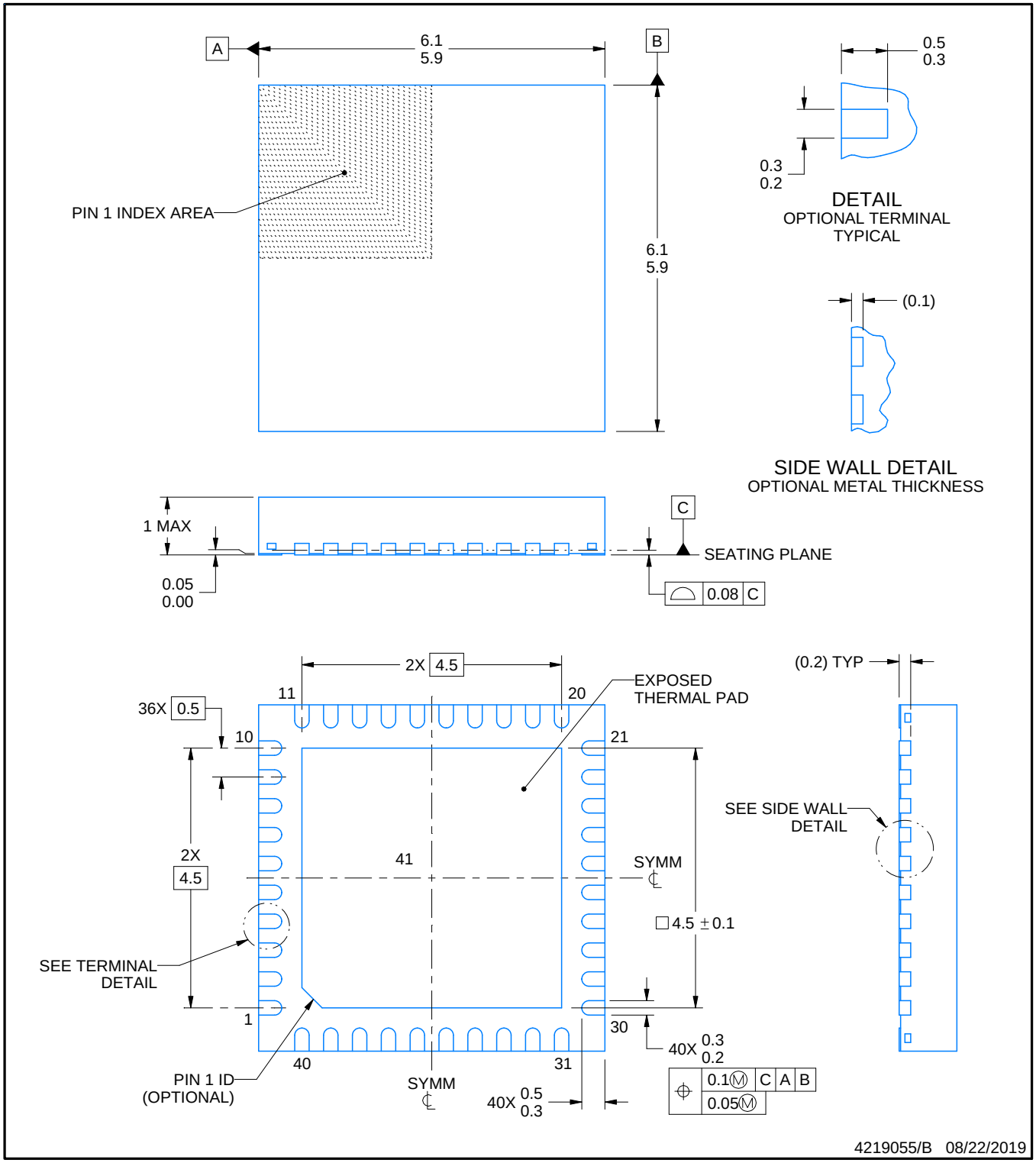
4225870/A

PACKAGE OUTLINE

RHA0040H

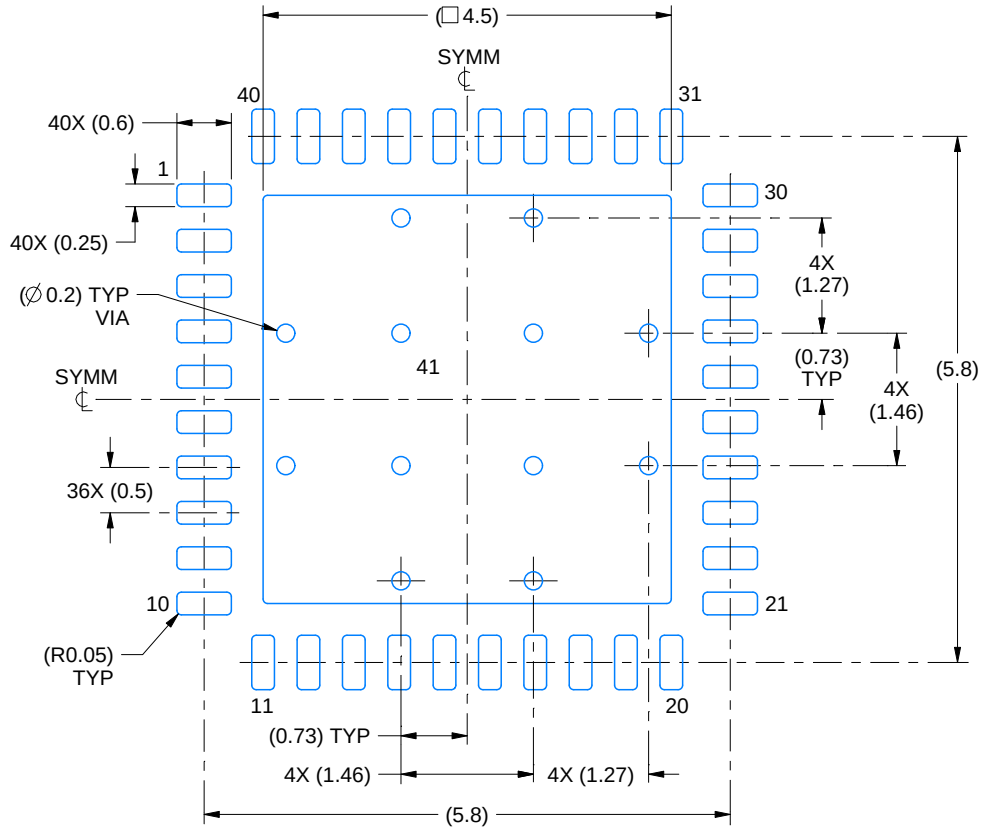
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

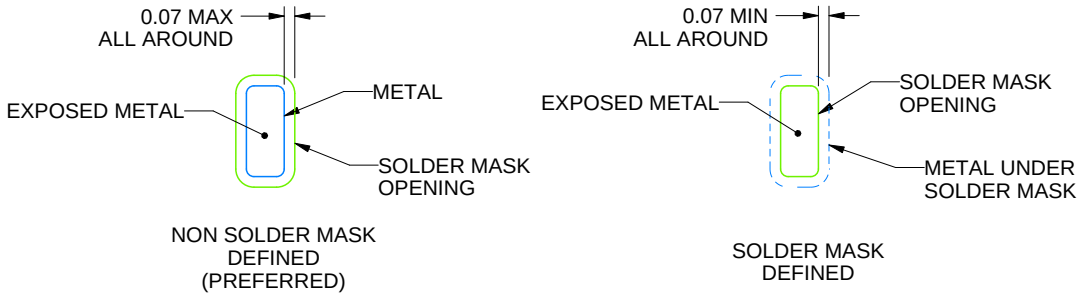


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

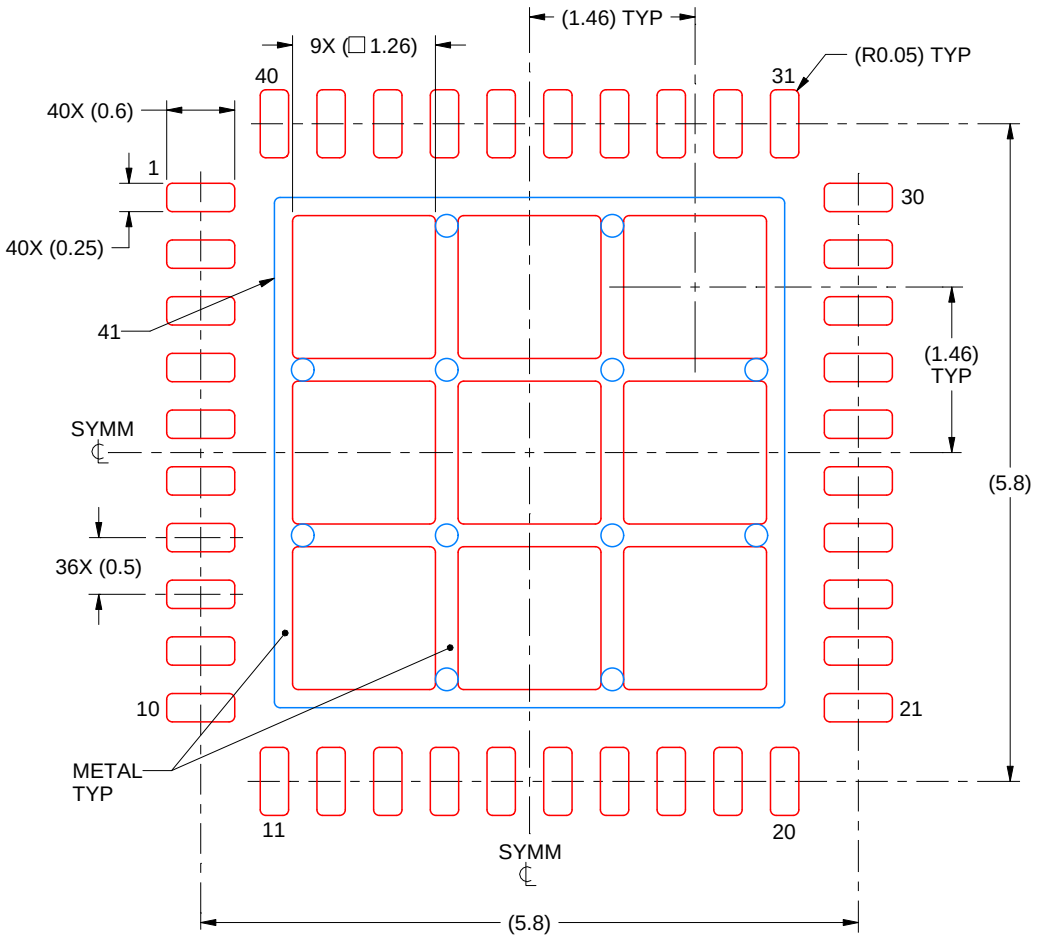


SOLDER MASK DETAILS

4219055/B 08/22/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
70% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

4219055/B 08/22/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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