ADS1283 高分解能アナログ/デジタル・コンバータ

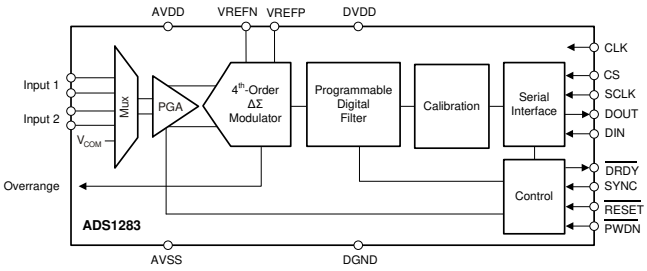
1 特長

- **高分解能**
  - SNR: 130dB (250SPS、PGA＝1)
- **高精度**
  - THD: -122dB
- **低消費電力**
  - 18mW (PGA＝1、2、4、8)
  - シャットダウン・モード: 10µW
- **低ノイズPGA**: 5nV/√Hz
- **2チャネルの入力マルチプレクサ**
- **本質的に安定な変調器と、高速応答の範囲外検出器**
- **柔軟なデジタル・フィルタ**:
  - Sinc + FIR + IIR (選択可能)
  - リニアまたは最小位相応答
  - プログラム可能なハイパス・フィルタ
  - FIRデータ・レートを選択可能: 250SPS～4kSPS
- **オフセットおよびゲイン較正エンジン**
- SYNC入力
- **アナログ電源**: 5Vまたは±2.5V
- **デジタル電源**: 1.8V～3.3V

2 アプリケーション

- **エネルギー調査**
- **地震モニタリング**
- **高精度の計測機器**

概略回路図



3 概要

ADS1283は非常に高性能な、シングル・チップのアナログ/デジタル・コンバータ(ADC)で、低ノイズのプログラマブル・ゲイン・アンプ(PGA)と2チャネルの入力マルチプレクサ(mux)が内蔵されています。ADS1283は、地震モニタリング機器の厳しい要求に適しています。

このコンバータは、4次の本質的に安定なデルタ-シグマ(ΔΣ)変調器を使用しており、ノイズおよび線形性の性能が非常に優れています。変調器のデジタル出力は、オンチップのデジタル・フィルタによってデジタル的にフィルタ処理およびデシメーションされ、ADC変換結果が生成されます。

柔軟な入力マルチプレクサにより、測定用の追加の外部入力と、内部の自己テスト入力接続を使用できます。PGAは非常に低ノイズで(5nV/√Hz)、入力インピーダンスが非常に高いため、広い範囲のゲインで、ジオフォンやハイドロフォンと簡単に接続できます。

デジタル・フィルタは、毎秒250～4000サンプル(SPS)のデータ・レートを選択できます。ハイパス・フィルタ(HPF)はコーナー周波数を設定可能です。オンチップのゲインおよびオフセットのスケーリング・レジスタが、システム較正をサポートします。

同期入力(SYNC)を使用して、複数のADS1283デバイスの変換を同期できます。

ADS1283は小型の24リード、5mm×4mm VQFNパッケージで供給され、-40℃～+85℃で完全に動作が規定されており、最大動作温度範囲は-50℃～+125℃です。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
ADS1283	VQFN (24)	5.00mm×4.00mm
ADS1283A		
ADS1283B		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

デバイスの比較

型番	オフセット・オプション	THD (TYP)	ゲイン
ADS1283	100mV	-122dB	1～64
ADS1283A	100mV	-118dB	1、4、16
ADS1283B	75mV、100mV	-122dB	1～64

目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision B (December 2017) から Revision C に変更 **Page**

- Web にフルバージョンをリリースするためにドキュメントを 変更 ... 1

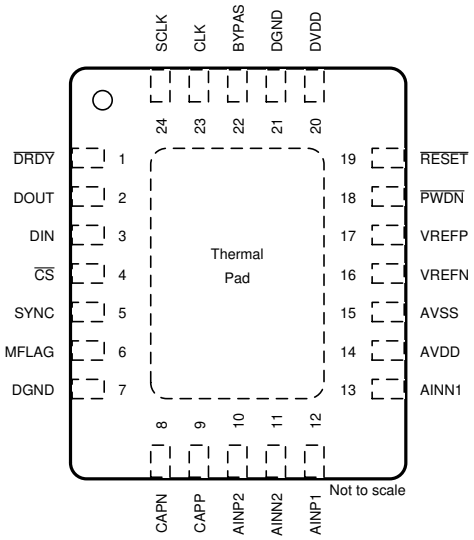
Revision A (May 2015) から Revision B に変更 **Page**

- データシートにADS1283Bデバイスと関連コンテンツを 追加 ... 1
- 「*製品情報*」および「*デバイスの比較*」表 追加 ... 1
- Added *Recommended Operating Conditions* table; content moved from *Electrical Characteristics* table. No values changed ... 5
- Deleted ADS1283A text from test condition in *Electrical Characteristic* table ... 6
- Added new row for ADS1283B test condition to *Offset* parameter in the *Electrical Characteristics* table ... 7
- Added *Switching Characteristics* table; content moved from *Timing Requirements* table. No values changed ... 9
- Changed text in *Offset* section for 75-mV option ... 22
- Changed Figure 45 to include CLK to SYNC timing ... 32
- Deleted t_{CSHD} and t_{SCSU} from Table 12 ... 32
- Added CLK to SYNC timing to Table 12 ... 32
- Changed text in last paragraph of *Pulse-Sync Mode* section ... 33
- Changed pulse-sync timing text to include CLK to SYNC timing ... 33
- Changed Figure 46 to include CLK to SYNC timing ... 33
- Changed opcode text of WREG command from 001 to 010 ... 47
- Added new OFFSET control bit to ID_CFG (register 00h) for ADS1283B device; no change to ADS1283 and ADS1283A functionality ... 48
- Changed format of register description tables ... 48

2014年1月発行のものから更新 **Page**

5 Pin Configuration and Functions

RHF Package
5-mm × 4-mm 24-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AINN1	13	Analog input	Negative analog input 1
AINN2	11	Analog input	Negative analog input 2
AINP1	12	Analog input	Positive analog input 1
AINP2	10	Analog input	Positive analog input 2
AVDD	14	Analog supply	Positive analog power supply
AVSS	15	Analog supply	Negative analog power supply
BYPAS	22	Analog	1.8-V sub-regulator output: connect 1-μF capacitor to DGND
CAPN	8	Analog	PGA output: connect 10-nF capacitor from CAPP to CAPN
CAPP	9	Analog	PGA output: connect 10-nF capacitor from CAPP to CAPN
CLK	23	Digital input	Master clock input (4.096 MHz)
$\overline{CS}$	4	Digital input	Serial interface chip select, active low
DGND	7	Ground	Digital ground (tie to digital ground plane)
DGND	21	Ground	Digital ground (tie to digital ground plane)
DIN	3	Digital input	Serial interface data input
DOUT	2	Digital output	Serial Interface data output
$\overline{DRDY}$	1	Digital output	Data ready output: active low
DVDD	20	Digital supply	Digital power supply: 1.65 V to 3.6 V
MFLAG	6	Digital output	Modulator overrange flag: 0 = normal, 1 = modulator overrange
$\overline{PWDN}$	18	Digital input	Power-down input, active low
$\overline{RESET}$	19	Digital input	Reset input, active low
SCLK	24	Digital input	Serial interface shift clock input
SYNC	5	Digital input	Synchronize input, rising edge active
VREFN	16	Analog input	Negative reference input
VREFP	17	Analog input	Positive reference input
Thermal pad			Do not electrically connect the thermal pad. The thermal pad must be soldered to PCB. Thermal pad vias are optional and can be removed.

6 Specifications

6.1 Absolute Maximum Ratings(1)

Over operating free-air temperature range (unless otherwise noted).

	MIN	MAX	UNIT
AVDD to AVSS	–0.3	5.5	V
AVSS to DGND	–2.8	0.3	V
DVDD to DGND	–0.3	3.9	V
Analog input voltage	AVSS – 0.3	AVDD + 0.3	V
Digital input voltage to DGND	–0.3	DVDD + 0.3	V
Input current, continuous	–10	10	mA
Operating temperature	–50	125	°C
Junction temperature		150	°C
Storage temperature, T_{stg}	–60	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
POWER SUPPLY					
AVSS	Negative analog supply (relative to DGND)	–2.6		0	V
AVDD	Positive analog supply (relative to AVSS)	AVSS + 4.75		AVSS + 5.25	V
DVDD	Digital supply (relative to DGND)	1.65		3.6	V
ANALOG INPUTS					
FSR	Full-scale input voltage range (V_{IN} = AINP – AINN)		±V_{REF} / (2 × PGA)		V
	Calibration margin(1)			106	%FSR
AINP or AINN	Absolute input voltage range	AVSS + 0.7		AVDD – 1.25	V
VOLTAGE REFERENCE INPUTS					
	Reference input voltage (V_{REF} = VREFP – VREFN)	1	5	(AVDD – AVSS) + 0.2	V
VREFN	Negative reference input	AVSS – 0.1		VREFP – 1	V
VREFP	Positive reference input	VREFN + 1		AVDD + 0.1	V
DIGITAL INPUTS					
V_{IH}	High-level input voltage	0.8 × DVDD		DVDD	V
V_{IL}	Low-level input voltage	DGND		0.2 × DVDD	V
f_{CLK}	Clock input	1		4.096	MHz
f_{SCLK}	Serial clock rate			f_{CLK} / 2	MHz
TEMPERATURE					
	Specified temperature	–40		85	°C

(1) Calibration margin is the maximum allowable input voltage after user calibration of offset and gain errors.

6.4 Thermal Information

THERMAL METRIC[1]		ADS1283 RHF (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

maximum and minimum specifications over –40°C to +85°C; typical specifications at 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, PGA = 1, OFFSET bit = 1 (enabled), CHOP bit = 1 (enabled), and f_{DATA} = 1000 SPS (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG INPUTS							
	PGA input voltage noise density				5		nV/√Hz
	Differential input impedance[1]	CHOP enabled			1		GΩ
		CHOP disabled			100		
	Common-mode input impedance				1		GΩ
I_{IB}	Input bias current				1		nA
	Crosstalk	f = 31.25 Hz			–135		dB
	Mux switch on-resistance	Each switch			30		Ω
PGA OUTPUT (CAPP, CAPN)							
	Absolute output range			AVSS + 0.4		AVDD – 0.4	V
	PGA differential output impedance				600		Ω
	Output impedance tolerance				±10%		
	External bypass capacitance				10	100	nF
	Modulator differential input impedance				55		kΩ
AC PERFORMANCE							
SNR	Signal-to-noise ratio[2]			120	124		dB
THD	Total harmonic distortion[3]	ADS1283, ADS1283B	PGA = 1, 2, 4, 8, 16		–122	–114	dB
			PGA = 32		–117	–110	
			PGA = 64		–114		
		ADS1283A	PGA = 1, 4, 16		–118	–106	
SFDR	Spurious-free dynamic range				123		dB

(1) PGA chop feature is disabled by setting CHOP bit = '0'. See Table 4
(2) Inputs shorted; see Table 1.
(3) Input signal = 31.25 Hz, –0.5 dBFS.

Electrical Characteristics (continued)

maximum and minimum specifications over –40°C to +85°C; typical specifications at 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, PGA = 1, OFFSET bit = 1 (enabled), CHOP bit = 1 (enabled), and f_{DATA} = 1000 SPS (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC PERFORMANCE							
	Resolution			31			Bits
f_{DATA}	Data rate	FIR filter mode		250		4000	SPS
		Sinc filter mode		8000		128,000	
	Offset(4)	OFFSET disabled			±50	±200	µV
		OFFSET disabled, CHOP disabled			300		
		OFFSET enabled		95 / PGA	100 / PGA	105 / PGA	mV
			ADS1283B only	70 / PGA	75 / PGA	80 / PGA	
	Offset after calibration(5)				1		µV
	Offset drift	CHOP enabled			0.03		µV/°C
		CHOP disabled			0.5		
	Gain error(6)			–1.5%	–1.0%	–0.5%	
	Gain error after calibration(5)				0.0002%		
	Gain drift	PGA = 1			2		ppm/°C
		PGA = 16			9		
	Gain matching(7)				0.3%	0.8%	
CMR	Common-mode rejection	f_{CM} = 60 Hz, 1.25 V_{PP}(8)		95	110		dB
PSR	Power-supply rejection	f_{PS} = 60 Hz, 100 mV_{PP}(8)	AVDD, AVSS	80	90		dB
			DVDD	90	115		
VOLTAGE REFERENCE INPUTS							
	Reference input impedance				85		kΩ
DIGITAL FILTER RESPONSE							
	Pass-band ripple					±0.003	dB
	Pass band (–0.01dB)				0.375 × f_{DATA}		Hz
	Bandwidth (–3dB)				0.413 × f_{DATA}		Hz
	High-pass filter corner			0.1		10	Hz
	Stop band attenuation(9)			135			dB
	Stop band				0.500 × f_{DATA}		Hz
	Group delay	Minimum phase filter(10)			5 / f_{DATA}		s
		Linear phase filter			31 / f_{DATA}		
	Settling time (latency)	Minimum phase filter			62 / f_{DATA}		s
		Linear phase filter			62 / f_{DATA}		

(4) Offset specification is input referred. The offset scales by the reference voltage (V_{REF}).
(5) Calibration accuracy is on the level of noise reduced by four (calibration averages 16 readings).
(6) The PGA output impedance and the modulator input impedance results in –1% systematic gain error.
(7) Gain match relative to gain = 1.
(8) f_{CM} is the input common-mode frequency. f_{PS} is the power-supply frequency.
(9) Input frequencies in the range of Nf_{CLK} / 1024 ± f_{DATA} / 2 (where N = 1, 2, 3...) can intermodulate with the modulator chopper clock (and N multiples). At these frequencies, intermodulation = –120 dB, typ.
(10) At dc; see Figure 42.

Electrical Characteristics (continued)

maximum and minimum specifications over –40°C to +85°C; typical specifications at 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, PGA = 1, OFFSET bit = 1 (enabled), CHOP bit = 1 (enabled), and f_{DATA} = 1000 SPS (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS/OUTPUTS						
V_{OH}	High-level output voltage	I_{OH} = 1 mA	0.8 × DVDD			V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA			0.2 × DVDD	V
I_{lkg}	Input leakage	0 < $V_{DIGITAL\ IN}$ < DVDD			±10	µA
POWER SUPPLY						
	AVDD, AVSS current	Operating PGA = 1, 2, 4, 8		3.2	5.5	|mA|
		Operating PGA = 16, 32, 64		4	6	
		Standby mode		1	15	|µA|
		Power-down mode		1	15	
	DVDD current	Operating		0.6	0.8	mA
		Standby mode		25	50	µA
		Power-down mode(11)		1	15	
	Power dissipation	Operating PGA = 1, 2, 4, 8		18	30	mW
		Operating PGA = 16, 32, 64		22	33	
		Standby mode		90	250	µW
		Power-down mode		10	125	

(11) CLK input stopped.

6.6 Timing Requirements

at T_A = –40°C to +85°C and DVDD = 1.65 V to 3.6 V (unless otherwise noted)

		MIN	MAX	UNIT
t_{CSSC}	$\overline{CS}$ low to SCLK high: setup time	40		ns
t_{SCLK}	SCLK period	2	16	1 / f_{CLK}
$t_{SPWH, L}$	SCLK pulse duration, high and low(1)	0.8	10	1 / f_{CLK}
t_{DIST}	DIN valid to SCLK high: setup time	50		ns
t_{DIHD}	Valid DIN to SCLK high: hold time	50		ns
t_{CSH}	$\overline{CS}$ high pulse	100		ns
t_{SCCS}	SCLK high to $\overline{CS}$ high	24		1/f_{CLK}

(1) Holding SCLK low for 64 $\overline{DRDY}$ falling edges resets the serial interface.

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CSDOD}	$\overline{CS}$ low to DOUT driven: propagation delay				60	ns
t_{DOPD}	SCLK low to valid new DOUT: propagation delay	Load on DOUT = 20 pF || 100 kΩ			100	ns
t_{DOHD}	SCLK low to DOUT invalid: hold time		0			ns
t_{CSDOZ}	$\overline{CS}$ high to DOUT tristate				40	ns

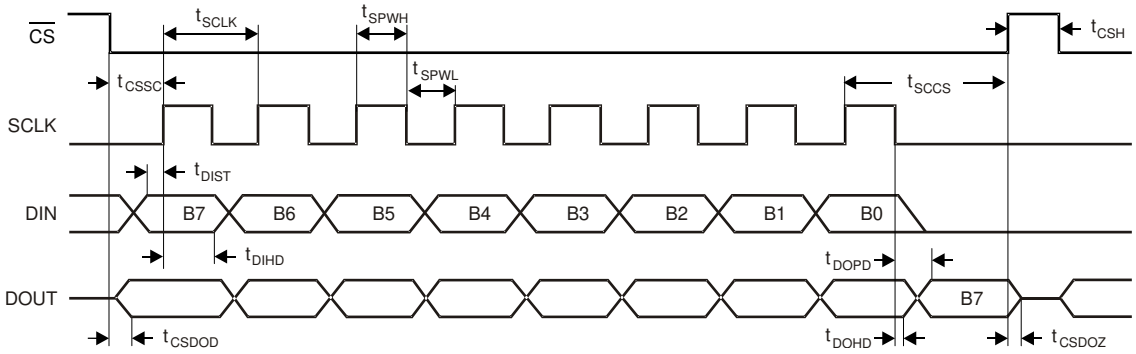


Figure 1. Serial Interface Timing Diagram

6.8 Typical Characteristics

At +25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, PGA = 1, OFFSET enabled, CHOP enabled, and f_{DATA} = 1000 SPS (unless otherwise noted). For ADS1283A, the electrical characteristics apply at PGA = 1, 4, and 16 only.

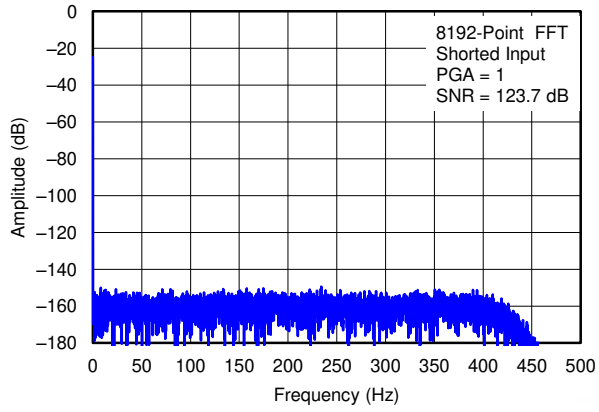


Figure 2. Output Spectrum

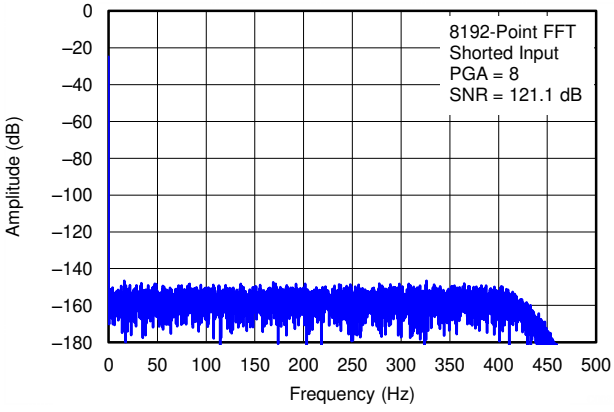


Figure 3. Output Spectrum

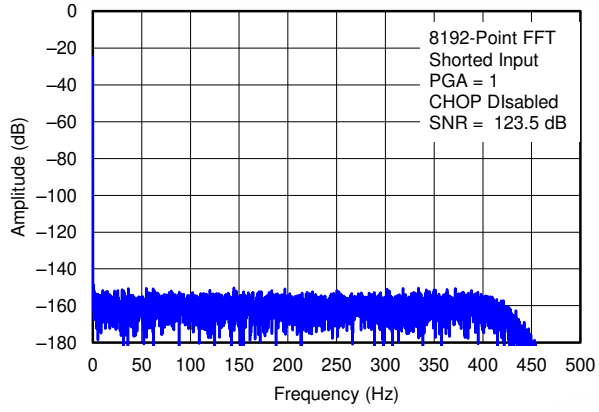


Figure 4. Output Spectrum

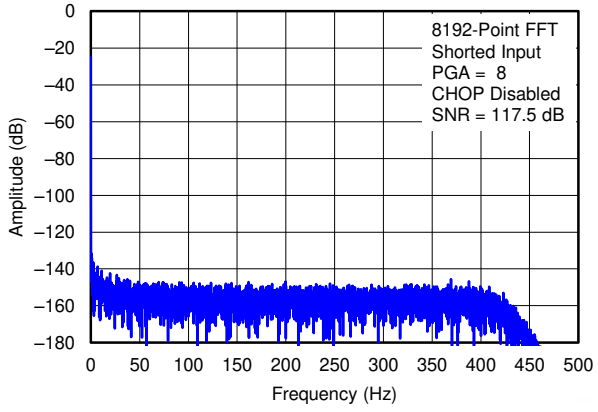


Figure 5. Output Spectrum

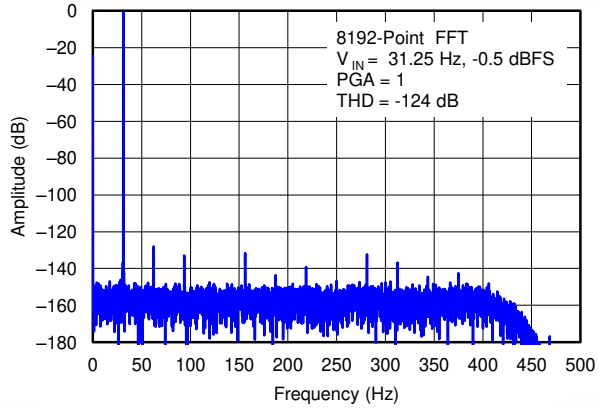


Figure 6. Output Spectrum

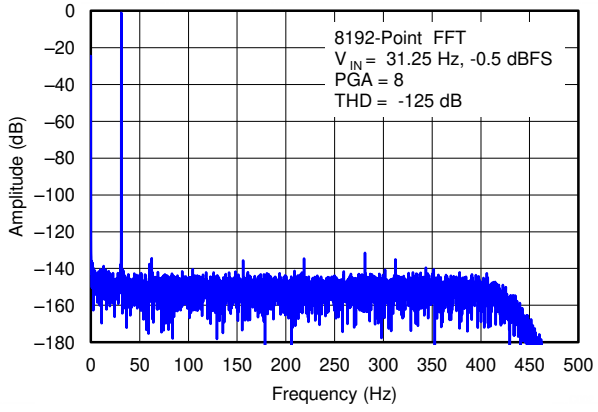


Figure 7. Output Spectrum

Typical Characteristics (continued)

At +25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, PGA = 1, OFFSET enabled, CHOP enabled, and f_{DATA} = 1000 SPS (unless otherwise noted). For ADS1283A, the electrical characteristics apply at PGA = 1, 4, and 16 only.

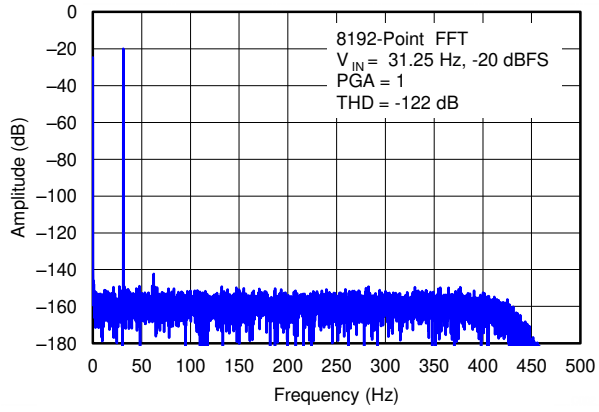


Figure 8. Output Spectrum

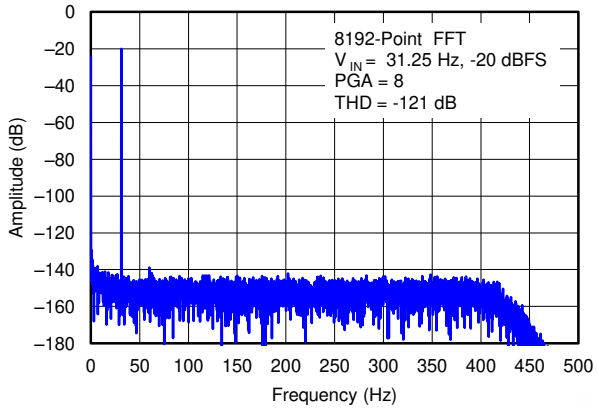


Figure 9. Output Spectrum

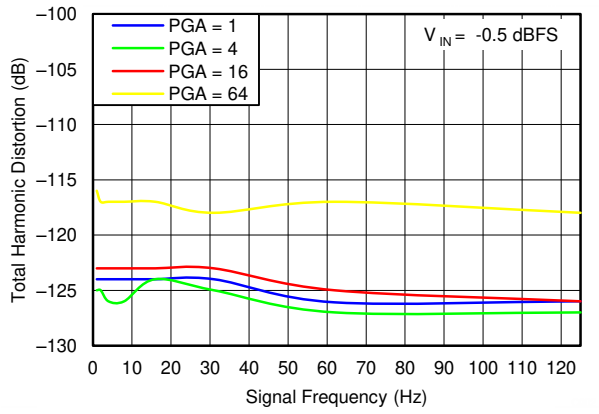


Figure 10. THD vs Signal Frequency

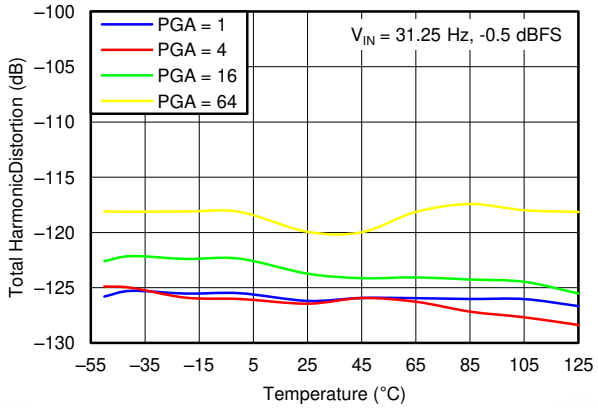


Figure 11. THD vs Temperature

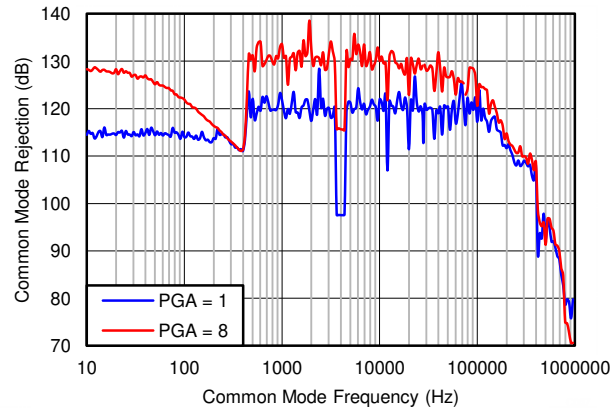


Figure 12. CMR vs Common-Mode Frequency

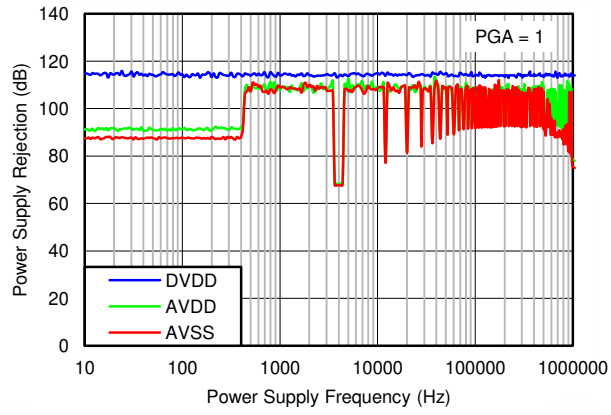


Figure 13. PSR vs Power-Supply Frequency

Typical Characteristics (continued)

At +25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, PGA = 1, OFFSET enabled, CHOP enabled, and f_{DATA} = 1000 SPS (unless otherwise noted). For ADS1283A, the electrical characteristics apply at PGA = 1, 4, and 16 only.

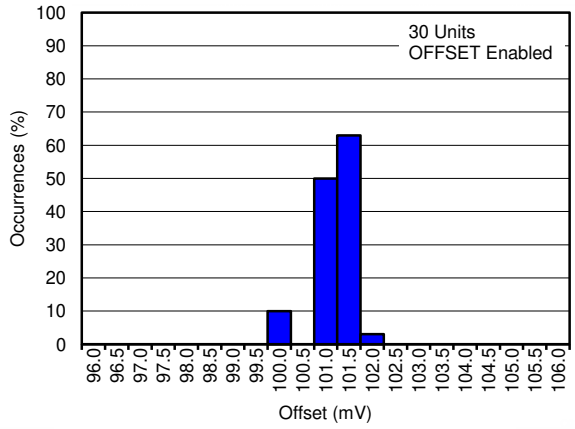


Figure 14. Offset-Voltage Histogram

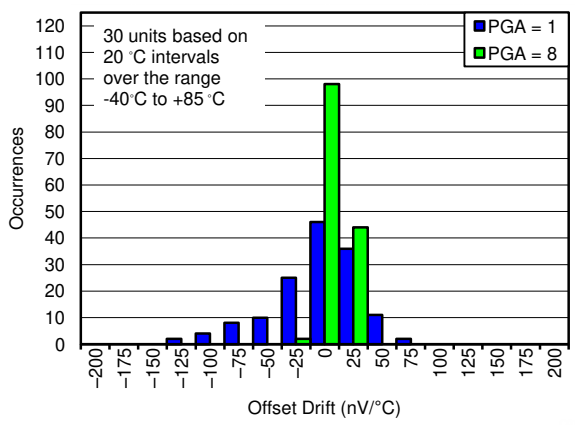


Figure 15. Offset-Voltage Drift Histogram

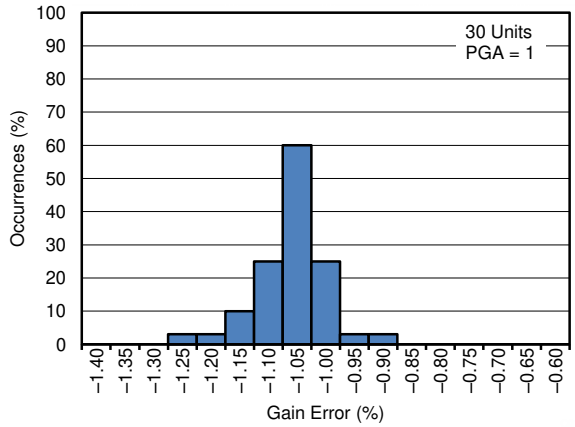


Figure 16. Gain-Error Histogram

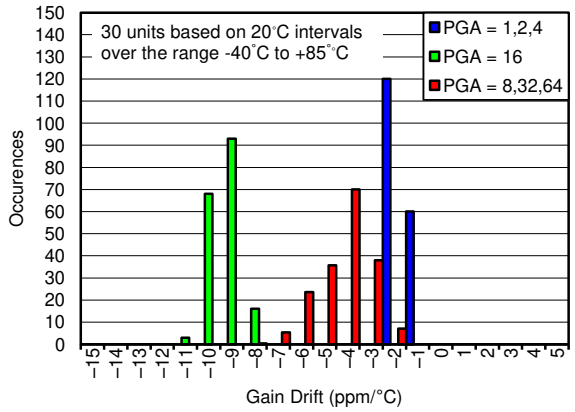


Figure 17. Gain-Error Drift Histogram

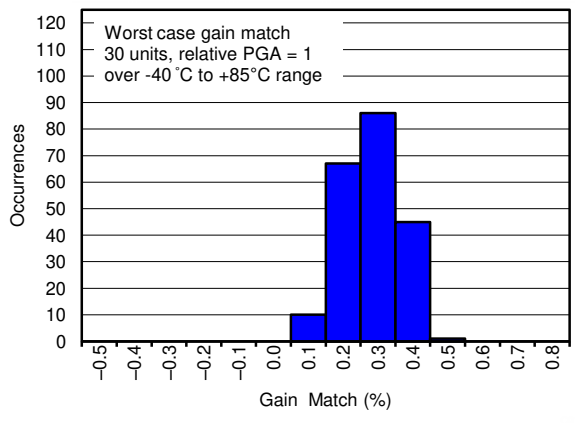


Figure 18. Gain-Match Histogram

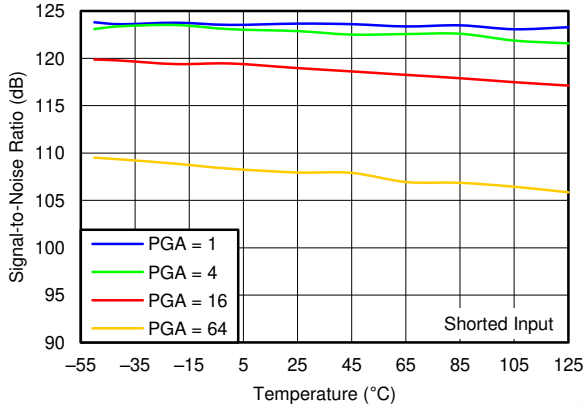


Figure 19. SNR vs Temperature

Typical Characteristics (continued)

At +25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, PGA = 1, OFFSET enabled, CHOP enabled, and f_{DATA} = 1000 SPS (unless otherwise noted). For ADS1283A, the electrical characteristics apply at PGA = 1, 4, and 16 only.

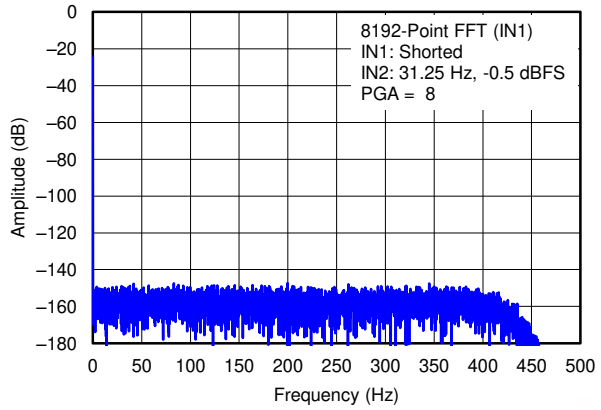


Figure 20. Crosstalk Output Spectrum

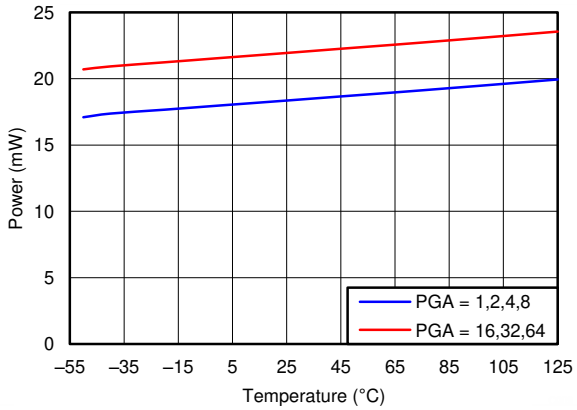


Figure 21. Power vs Temperature

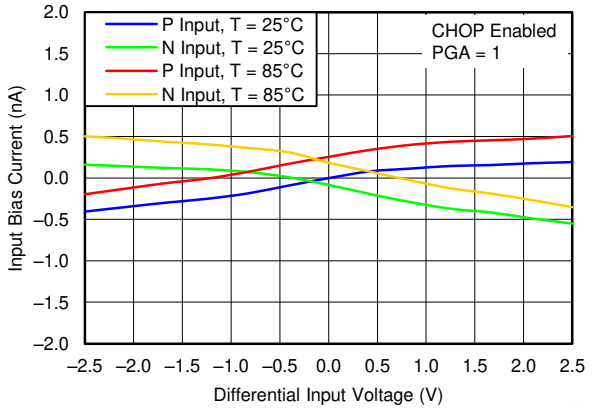


Figure 22. Input Bias Current vs Input Voltage

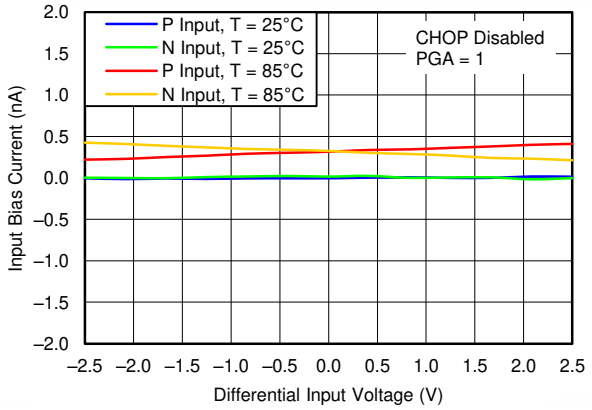


Figure 23. Input Bias Current vs Input Voltage

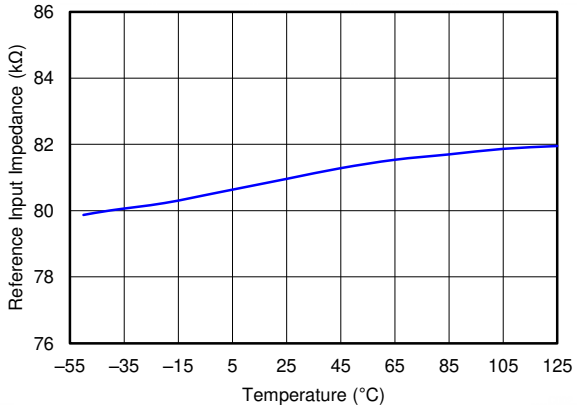


Figure 24. Reference Input Impedance vs Temperature

7 Parameter Measurement Information

7.1 Noise Performance

The ADS1283 offers outstanding signal-to-noise ratio (SNR). The SNR depends on the ADC data rate and the PGA gain selected. As the bandwidth is reduced by decreasing the data rate, the SNR improves correspondingly. Similarly, as gain is increased, the input-referred noise decreases. The PGA noise is independent of gain; therefore, as the gain increases, the input range correspondingly decreases, resulting in decreased SNR.

The ADS1283 provides a *chop* feature that reduces the PGA 1/f noise. See the *Programmable Gain Amplifier (PGA)* section for more information about chopping. Table 1 summarizes the SNR and input noise voltage with the CHOP bit enabled. Disabling the CHOP bit results in increased low-frequency noise, particularly evident with high PGA gains and lower sample rates. Table 2 summarizes SNR and input noise voltage with CHOP disabled.

Table 1. Signal-to-Noise Ratio (dB) and Input Noise (μV), CHOP Bit Enabled

DATA RATE (SPS)	PGA (SNR, dB)(1)							PGA (Input-Referred Noise, μV RMS)						
	1	2	4	8	16	32	64	1	2	4	8	16	32	64
250	130	129	129	127	125	119	114	0.59	0.30	0.16	0.10	0.07	0.06	0.06
500	127	126	126	124	122	116	111	0.84	0.43	0.23	0.14	0.09	0.09	0.08
1000	124	123	123	121	119	113	108	1.19	0.60	0.32	0.20	0.13	0.12	0.11
2000	121	120	120	118	116	110	105	1.68	0.86	0.46	0.28	0.18	0.17	0.16
4000	117	117	117	115	113	107	102	2.40	1.22	0.66	0.40	0.26	0.25	0.23

(1) Typical values at T = +25°C and V_{REF} = 5 V. SNR values rounded to the nearest dB. Number of ADC conversions used in the analysis varied to maintain measurement bandwidth = 0.1 Hz to 0.413 × data rate. Note that SNR and input noise data of ADS1283A applies to PGA = 1, 4, and 16 only.

Table 2. Signal-to-Noise Ratio (dB) and Input Noise (μV), CHOP Bit Disabled

DATA RATE (SPS)	PGA (SNR, dB)(1)							PGA (Input-Referred Noise, μV RMS)						
	1	2	4	8	16	32	64	1	2	4	8	16	32	64
250	129	128	125	120	116	110	104	0.63	0.37	0.26	0.21	0.18	0.17	0.18
500	126	125	123	119	114	108	103	0.87	0.47	0.31	0.25	0.21	0.21	0.20
1000	123	123	121	117	114	108	102	1.20	0.65	0.39	0.30	0.22	0.22	0.22
2000	120	120	119	116	112	107	101	1.69	0.91	0.51	0.37	0.26	0.25	0.25
4000	117	117	116	114	111	105	99	2.41	1.24	0.70	0.46	0.33	0.31	0.30

(1) Typical values at T = +25°C and V_{REF} = 5 V. SNR values rounded to the nearest dB. Number of ADC conversions used in the analysis varied to maintain measurement bandwidth = 0.1 Hz to 0.413 × data rate. Note that SNR and input noise data of ADS1283A applies to PGA = 1, 4, and 16 only.

Input-referred noise is related to SNR by Equation 1:

$$SNR = 20\log \frac{FSR_{RMS}}{N_{RMS}}$$

where

- FSR_{RMS} = Full-scale range RMS = V_{REF} / (2 × $\sqrt{2}$ × PGA)
- N_{RMS} = Noise (RMS, input-referred) (1)

8 Detailed Description

8.1 Overview

The ADS1283 is a high-performance analog-to-digital converter (ADC) intended for energy exploration, seismic monitoring, chromatography, and other exacting performance applications. The converter provides 31-bit resolution in data rates from 250 SPS to 4000 SPS. See the *Functional Block Diagram* section for a block diagram of the ADS1283.

The ADS1283A device is functionally equivalent to the ADS1283, except that the ADS1283A supports PGA gains of 1, 4, and 16 only. The ADS1283A also relaxes the THD specification of these gains. See the *Electrical Characteristics* section for more details. The ADS1283B provides equivalent performance to the ADS1283, but provides two offset voltage options, 75 mV and 100 mV. See Offset for details.

The two-channel input mux allows five configurations:

1. Input 1
2. Input 2
3. Input 1 and input 2 shorted together
4. Input 1 and input 2 disconnected and PGA input internally shorted with two 400-Ω resistors
5. Input 1 and input 2 shorted to perform input common-mode test

See the *Analog Inputs and Multiplexer* section for more details.

The input mux is followed by a continuous-time PGA, featuring very low noise of 5 nV/$\sqrt{\text{Hz}}$. The PGA is controlled by register settings, allowing gains from 1 to 64 for the ADS1283 and ADS1283B, and gains of 1, 4, and 16 for the ADS1283A.

The inherently-stable, fourth-order, delta-sigma modulator measures the differential input signal (V_{IN} = AINP – AINN) against the differential reference (V_{REF} = VREFP – VREFN). A digital output (MFLAG) indicates that the modulator is in overload as a result of an overdrive condition. The modulator connects to the on-chip digital filter that provides the output codes.

The digital filter consists of a variable decimation rate, fifth-order sinc filter, followed by a variable phase, decimate-by-32, finite-impulse response (FIR) low-pass filter with programmable phase, and then by an adjustable high-pass filter for dc removal of the output code. The output of the digital filter can be taken from the sinc or the FIR low-pass, with the FIR option of the infinite impulse response (IIR) high-pass section.

Gain and offset registers scale the digital filter output to produce the final code value. The scaling feature can be used for calibration and sensor gain matching.

The SYNC input resets the operation of both the digital filter and the modulator, allowing synchronization conversions of multiple ADS1283 devices to an external event. The SYNC input supports a continuously-toggled input mode that accepts an external data frame clock locked to the conversion rate.

The $\overline{\text{RESET}}$ input resets the register settings and also restarts the conversion process.

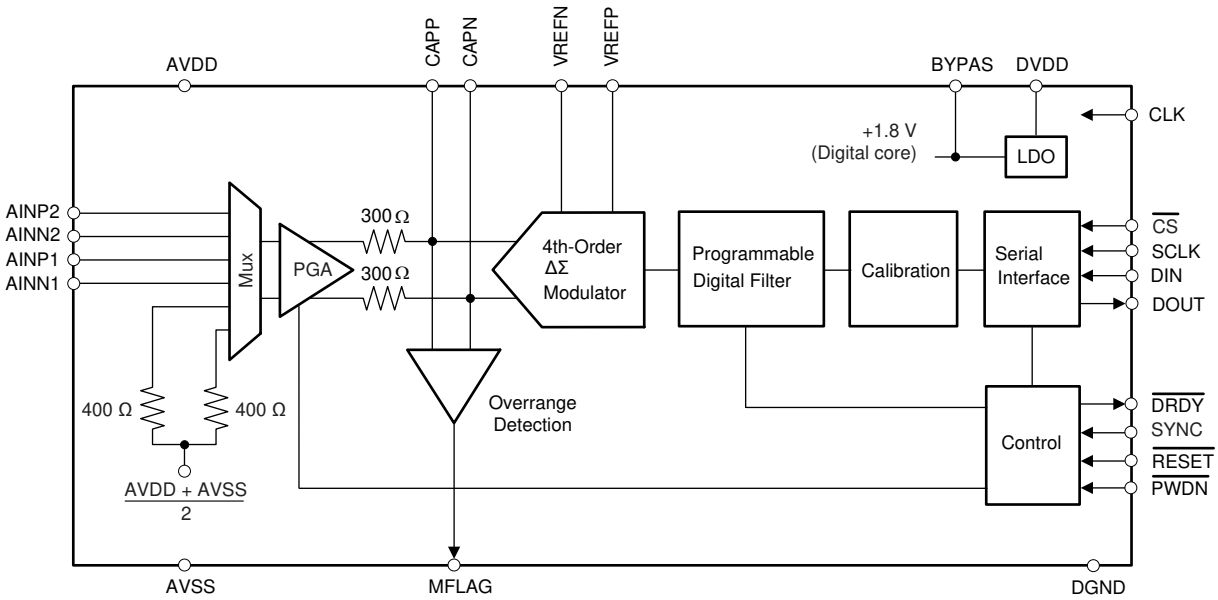
The $\overline{\text{PWDN}}$ input sets the device into a micro-power state. Note that register settings are not retained in $\overline{\text{PWDN}}$ mode. Use the STANDBY command in its place if it is desired to retain register settings (the quiescent current in standby mode is slightly higher).

Noise-immune Schmitt-trigger and clock-qualified inputs ($\overline{\text{RESET}}$ and SYNC) provide increased reliability in high-noise environments. The SPI™-compatible serial interface is used to read conversion data, in addition to reading from and writing to the configuration registers.

The device allows either unipolar and bipolar analog power-supply operation. The analog supplies may be set to +5 V for unipolar signals (with the inputs level shifted externally), or set to ±2.5 V to accept true bipolar input signals (ground referenced). The digital supply is separate and accepts voltages from 1.8 V to 3.3 V, independent of the analog power supplies used.

An internal subregulator is used to supply the digital core from DVDD. BYPAS (pin 28), is the subregulator output and requires a 1-μF capacitor for noise reduction. Note that the regulated output voltage on BYPAS is not available to drive external circuitry.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Analog Inputs and Multiplexer

A diagram of the input multiplexer is shown in Figure 25.

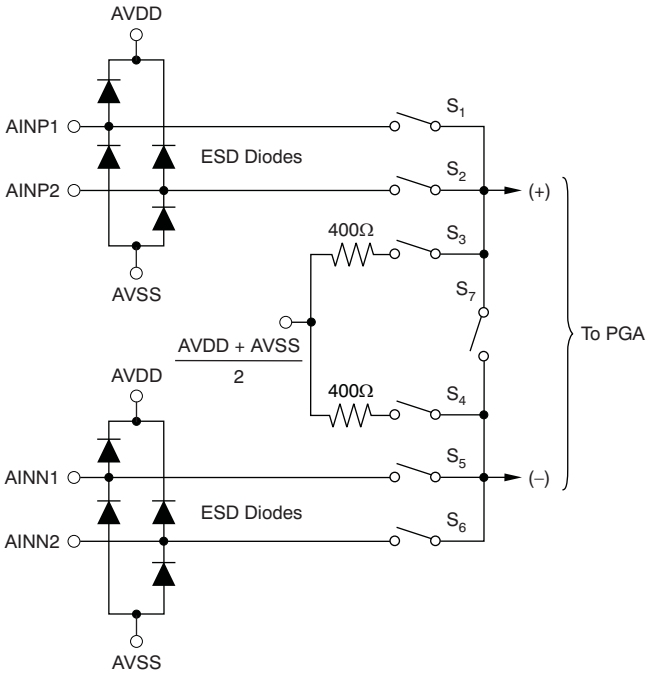


Figure 25. Analog Inputs and Multiplexer

ESD diodes protect the multiplexer inputs. If either input is taken below AVSS – 0.3 V, or above AVDD + 0.3 V, the ESD protection diodes can turn on. If these conditions are possible, use external clamp diodes, series resistors, or both to limit the input current to safe values (see the Absolute Maximum Ratings table).

Feature Description (continued)

Also, overdriving one unused input can affect the conversions of the other input. If an overdriven input interacts with the measured input, clamp the overdriven signal with external Schottky diodes.

The specified input operating range of the PGA is shown in Equation 2:

$$AVSS + 0.7V < (AINN \text{ or } AINP) < AVDD - 1.25V \quad (2)$$

For best operation, maintain absolute input levels (input signal level and common-mode level) within these limits.

The multiplexer connects one of the two external differential inputs to the preamplifier inputs, in addition to internal connections for various self-test modes. Table 3 summarizes the multiplexer configurations for Figure 25.

Table 3. Multiplexer Modes

MUX[2:0]	SWITCHES	DESCRIPTION
000	S_1, S_5	AINP1 and AINN1 connected to preamplifier
001	S_2, S_6	AINP2 and AINN2 connected to preamplifier
010	S_3, S_4	Preamplifier inputs shorted together through 400-Ω internal resistors
011	S_1, S_5, S_2, S_6	AINP1, AINN1 and AINP2, AINN2 connected together and to the preamplifier
100	S_6, S_7	External short, preamplifier inputs shorted to AINN2 (common-mode test)

The typical on-resistance (R_{ON}) of the multiplexer is 30 Ω (each switch). When the multiplexer is used to drive an external load on one input by a signal generator on the other input, on-resistance and on-resistance amplitude dependency can lead to measurement errors. Figure 26 shows THD versus load resistance and amplitude. THD improves with high-impedance loads and with lower-amplitude drive signals. The data are measured with the circuit from Figure 27 with MUX[2:0] = 011.

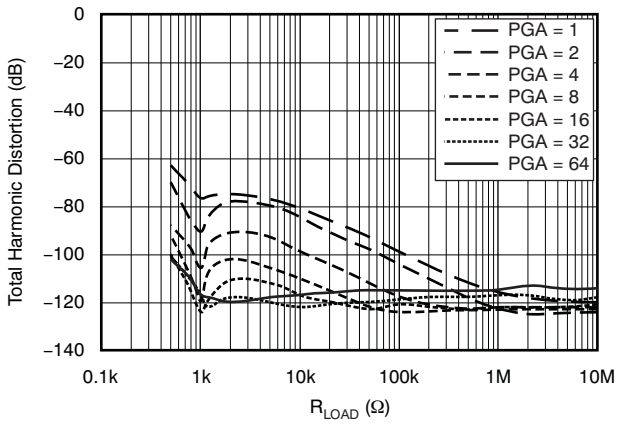


Figure 26. THD vs External Load and Signal Magnitude (PGA); See Figure 27

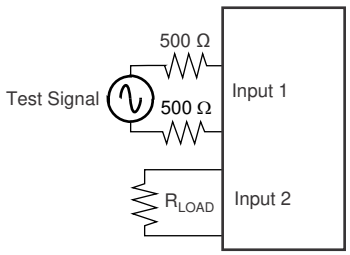


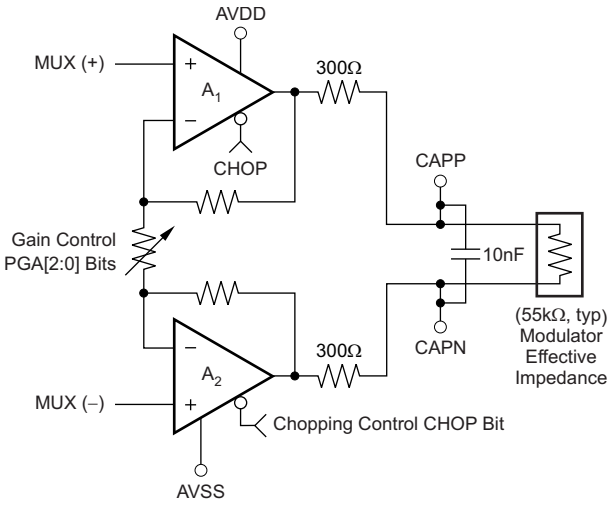
Figure 27. Driving an External Load Through the Multiplexer

8.3.2 Programmable Gain Amplifier (PGA)

The PGA of the ADS1283 is a low-noise, continuous-time, differential-in and differential-out CMOS amplifier. The gain is set by register bits PGA[2:0], and is programmable from 1 to 64 for the ADS1283, or can be set to 1, 4, and 16 for the ADS1283A. The PGA differentially drives the modulator through 300-Ω internal resistors. A C0G capacitor (10-nF C0G or film dielectric) must be connected to CAPP and CAPN to filter modulator sampling glitches. The external capacitor also serves as an antialias filter. The corner frequency is given in Equation 3:

$$f_P = \frac{1}{6.3 \times 600 \times C} \quad (3)$$

The ADS1283 PGA provides a chop feature. As shown in Figure 28, amplifiers A_1 and A_2 are chopper stabilized to remove the offset, offset drift, and 1/f noise. Chopper stabilization (or chopping) moves the offset and noise to f_{CLK} / 1024 (4 kHz, f_{CLK} = 4.096 MHz), which is located safely out of the pass-band frequency. Chopping can be disabled by setting the CHOP bit = 0. When chopping is disabled, the PGA input impedance increases (see *Differential Input Impedance* parameter in the Electrical Characteristics). As shown in Figure 29, chopping maintains flat noise density, leaving predominantly white noise. However, if chopping is disabled, the PGA input noise results in a rising 1/f noise profile.



(1) Modulator input impedance scales with clock rate.

Figure 28. PGA Block Diagram

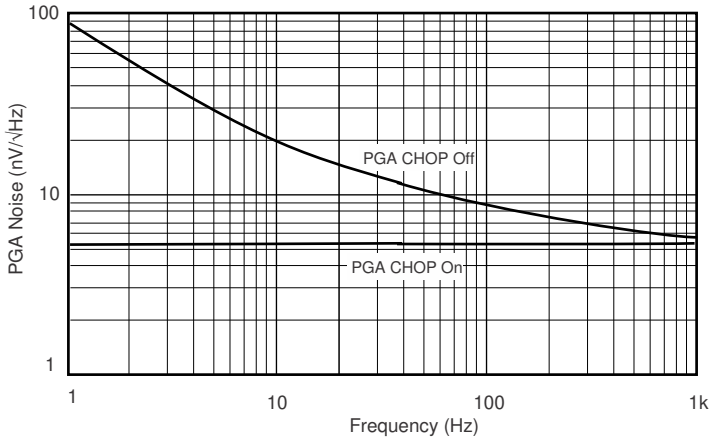


Figure 29. PGA Noise

As a result of the stray capacitance of the input chopping switches, low-level transient currents flow through the inputs when chopping is enabled. The average value of the transient currents versus the input voltage results in an effective input impedance. The effective input impedance depends on the PGA gain, as shown in Table 4. Despite the relatively high input impedance, carefully evaluate applications with high-impedance sensors or high-impedance termination resistors when chopping is enabled. Table 4 shows the PGA differential input impedance with CHOP enabled.

Table 4. Differential Input Impedance (CHOP Enabled)

PGA	DIFFERENTIAL INPUT IMPEDANCE (GΩ)
1	7
2	7
4	4
8	3
16	2
32	1
64	0.5

The PGA has programmable gains from 1 to 64. Table 5 shows the register bit setting for the PGA and resulting full-scale differential range.

Table 5. PGA Gain Settings

PGA[2:0]	GAIN(1)	DIFFERENTIAL INPUT RANGE (V)(2)
000	1	±2.5
001	2	±1.25
010	4	±0.625
011	8	±0.312
100	16	±0.156
101	32	±0.078
110	64	±0.039

(1) The ADS1283A supports gains of 1, 4, and 16 only.
(2) V_{REF} = 5 V. The input range scales with V_{REF}.

The specified range of the PGA output is shown in Equation 4:

$$AVSS + 0.4V < (CAPN \text{ or } CAPP) < AVDD - 0.4V \quad (4)$$

For best performance, maintain PGA output levels (signal + common-mode) within these limits.

8.3.3 Analog-to-Digital Converter (ADC)

The ADC block of the ADS1283 is composed of two sections: a high-accuracy modulator and a programmable digital filter.

8.3.3.1 Modulator

The high-performance modulator is an inherently-stable, fourth-order, ΔΣ, 2 + 2 pipelined structure, as Figure 30 shows. The modulator shifts the quantization noise to a higher frequency (out of the pass band), where the noise can be easily removed by digital filtering. The modulator data can either be completely filtered by the on-chip digital filter or partially filtered by the onboard sinc filter in conjunction with external, post-processing filters.

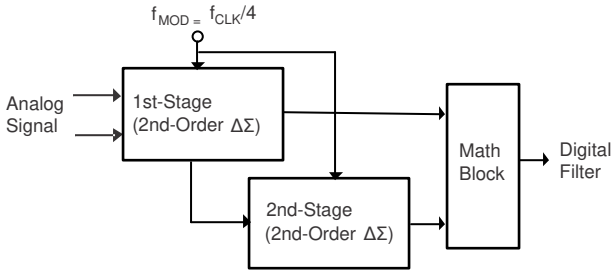


Figure 30. Fourth-Order Modulator

The modulator performance is optimized for input signals over the dc to 2-kHz bandwidth. As Figure 31 shows, the effect of PGA and modulator chop result in spectral artifacts at the chop frequency (4 kHz) and related odd-order harmonics to the chop frequency. When using the sinc filter mode in conjunction with an external post-decimation filter, design the external digital filter to suppress the modulator chopping artifacts.

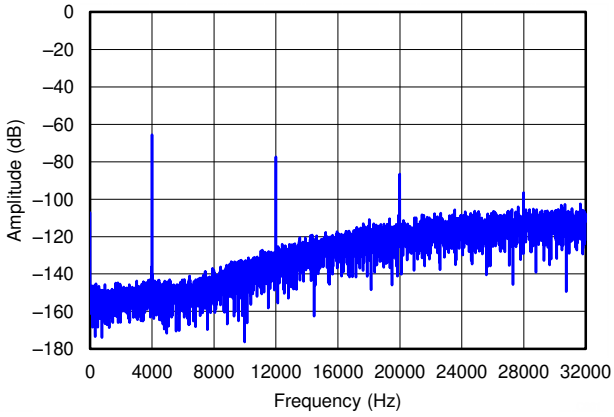


Figure 31. Sinc Output FFT (64 kSPS)

8.3.3.1.1 Modulator Overrange

The ADS1283 modulator is inherently stable, and therefore, has predictable recovery behavior resulting from an input overdrive condition. The modulator does not exhibit self-reset cycles, which often results in an unstable output data stream. The ADS1283 modulator outputs a data stream with 90% duty cycle of ones-to-zeroes density with the positive full-scale input signal applied (10% duty cycle with the negative full-scale signal). If the input is overdriven past 90% modulation, but below 100% modulation (10% and 0% for negative overdrive, respectively), the modulator remains stable and continues to output the 1s density data stream. The digital filter may or may not clip the output codes to +FS or –FS, depending on the duration of the overdrive. When the input returns to the normal range from a long-duration overdrive (worst case), the modulator returns immediately to the normal range, but the group delay of the digital filter delays the return of the conversion result to within the linear range (31 readings for linear phase FIR). An additional 31 readings (62 total) are required for completely-settled data.

If the inputs are sufficiently overdriven to drive the modulator to full duty cycle (that is, all 1s or all 0s), the modulator enters a stable saturated state. The digital output code may clip to +FS or –FS, again depending on the duration. A small-duration overdrive condition may not always clip the output code. When the input returns to the normal range, the modulator requires up to 12 modulator clock cycles (f_{MOD}) to exit saturation and return to the linear region. The digital filter requires an additional 62 conversions for fully-settled data (linear-phase FIR).

In the extreme case of input overrange (where either overdriven input exceeds the voltage of the analog supply voltage plus an internal ESD diode drop), the internal diodes begin to conduct, thus clipping the input signal. When the input overdrive is removed, the diodes recover quickly. Make sure to limit the input current to 10 mA (continuous duty) if an overvoltage condition is possible.

8.3.3.1.2 Modulator Input Impedance

The modulator samples the buffered input voltage with an internal capacitor to perform conversions. The charging of the input sampling capacitor draws a transient current from the PGA output. Use the average value of the current to calculate an effective input impedance, as shown in Equation 5:

$$R_{EFF} = 1 / (f_{MOD} \times C_S) \quad (5)$$

where

- f_{MOD} = Modulator sample frequency = CLK / 4
- C_S = Input sampling capacitor = 17 pF (typ)

The resulting modulator input impedance is 55 kΩ (CLK = 4.096 MHz). The modulator input impedance and the internal PGA 300-Ω output resistors result in a systematic gain error of –1%. The modulator C_S can vary ±20% over production lots, affecting the nominal gain error.

8.3.3.1.3 Modulator Overrange Detection (MFLAG)

The ADS1283 has a fast-responding, overrange detection that indicates when the differential input exceeds 100% or –100% full-scale. The threshold tolerance is ±2.5%.The MFLAG output pin asserts high when in an overrange condition. As Figure 32 and Figure 33 illustrate, the absolute differential input is compared to 100% of range. The output of the comparator is sampled at the rate of f_{MOD} / 2, yielding the MFLAG output. The minimum detectable MFLAG pulse duration is f_{MOD} / 2.

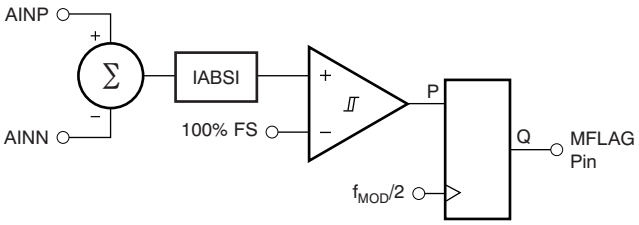


Figure 32. Modulator Overrange Block Diagram

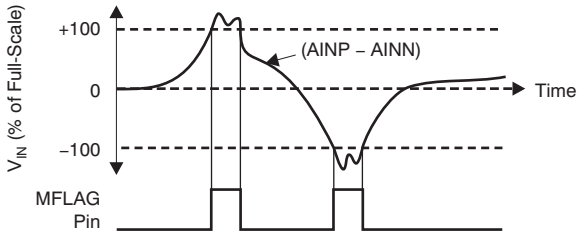


Figure 33. Modulator Overrange Flag Operation

8.3.3.1.4 Offset

The ADC modulator can produce low-level idle tones that appear in the spectrum when there is no signal input or when low-level signal inputs are present to the ADC. The ADC provides an optional dc offset voltage designed to shift the idle tones to the stop band of digital filter response, where the idle tones are reduced. The internal offset is applied to the modulator input; therefore, the offset voltage amplitude is independent of PGA gain. For all ADS1283 versions, the offset option is 100 mV. For the ADS1283B, a second offset option is 75 mV. The 75-mV offset optimally reduces idle tones under various gain, data rate, and chop mode settings.

The offset is enabled by the OFFSET1 and OFFSET0 bits (default is off). The offset voltage reduces the available input range 4% (3% for the 75 mV value) before the onset of clipped codes. The offset voltage can be calibrated by using the offset calibration register (OFC[2:0]). Use the offset calibration register to compensate the offset voltage, thereby restoring the full input voltage range. See *Offset and Full-Scale Calibration Registers* and *Calibration Commands (OFSCAL and GANCAL)* sections for more details.

8.3.3.1.5 Voltage Reference Inputs (VREFP, VREFN)

The voltage reference for the ADS1283 is the differential voltage between VREFP and VREFN:

$$V_{REF} = VREFP - VREFN \quad (6)$$

The reference inputs use a structure similar to that of the analog inputs with the circuitry of the reference inputs shown in Figure 34. The average load presented by the switched-capacitor reference input can be modeled with an effective differential impedance of:

$$R_{EFF} = t_{SAMPLE} / C_{IN} \ (t_{SAMPLE} = 1 / f_{MOD}). \quad (7)$$

Note that the effective impedance of the reference inputs loads the external reference.

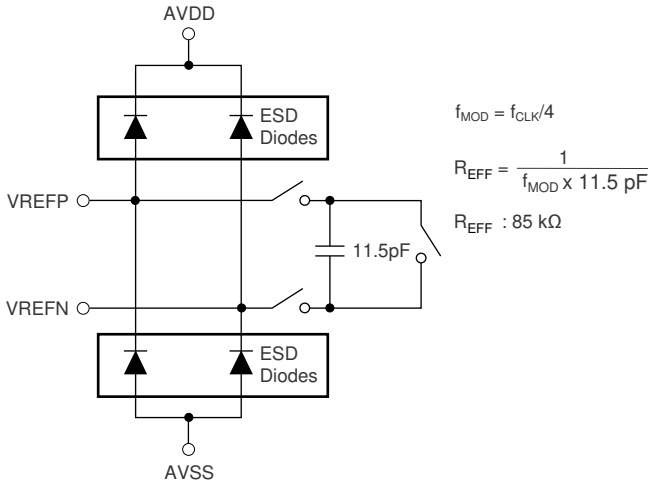


Figure 34. Simplified Reference Input Circuit

Place a 0.1-µF ceramic capacitor directly between the ADC VREFP and VREFN pins. Multiple ADC applications can share a single voltage reference, but must have individual capacitors placed for each ADC.

The ADS1283 reference inputs are protected by ESD diodes. In order to prevent these diodes from turning on, the voltage on either input must stay within the range shown in Equation 8:

$$AVSS - 300mV < (VREFP \text{ or } VREFN) < AVDD + 300mV \quad (8)$$

The minimum valid input for VREFN is AVSS – 0.1 V, and the maximum valid input for VREFP is AVDD + 0.1 V.

To achieve the best performance from the ADS1283, use a high-quality 5-V reference voltage. A 4-V or 4.5-V reference voltage can be used; however, this lower reference voltage reduces the signal input range with a corresponding decrease of SNR. Noise and drift on the reference degrade overall system performance. To achieve optimum performance, make sure to give special care to the circuitry generating the reference voltages. See the *Application Information* section for reference recommendations.

8.3.3.2 Digital Filter

The digital filter receives the modulator output and decimates the data stream. By adjusting the amount of filtering, tradeoffs can be made between resolution and data rate: filter more for higher resolution, filter less for higher data rate.

The digital filter is comprised of three cascaded filter stages: a variable-decimation, fifth-order sinc filter; a fixed-decimation FIR, low-pass filter (LPF) with selectable phase; and a programmable, first-order, high-pass filter (HPF), as shown in Figure 35.

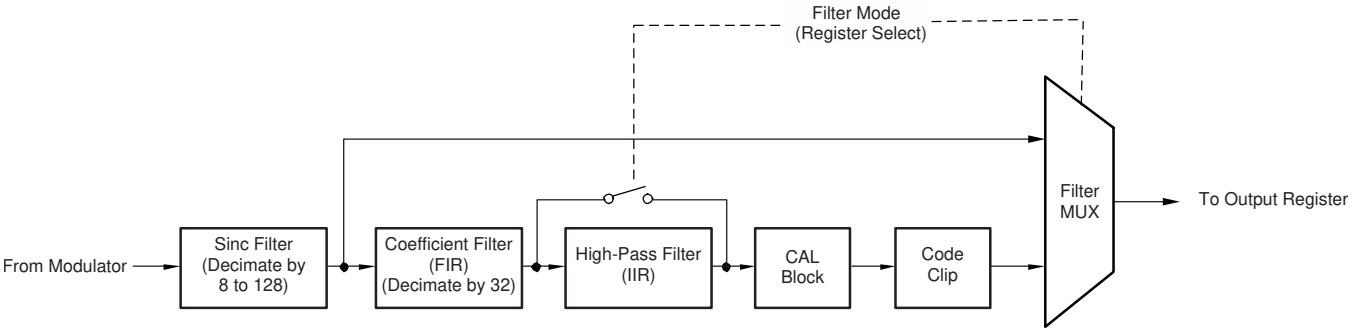


Figure 35. Digital Filter and Output Code Processing

The output can be taken from one of the three filter blocks, as Figure 35 shows. For partial filtering by the ADS1283, select the sinc filter output. For complete on-chip filtering, activate both the sinc + FIR stages. The HPF can then be included to remove dc and low frequencies from the data. Table 6 shows the filter options.

Table 6. Digital Filter Selection

FILTR[1:0] BITS	DIGITAL FILTERS SELECTED
00	Reserved (not used)
01	Sinc
10	Sinc + FIR
11	Sinc + FIR + HPF (low-pass and high-pass)

8.3.3.2.1 Sinc Filter Stage (sinx / x)

The sinc filter is a variable decimation rate, fifth-order, low-pass filter. Data are supplied to this section of the filter from the modulator at the rate of f_{MOD} (f_{CLK} / 4). The sinc filter attenuates the high-frequency noise of the modulator, then decimates the data stream into parallel data. The decimation rate affects the overall data rate of the converter, and is set by the DR[2:0] register bits, as shown in Table 7.

Table 7. Sinc Filter Data Rates

DR[2:0] REGISTER	DECIMATION RATIO (N)	DATA RATE (SPS)
000	128	8,000
001	64	16,000
010	32	32,000
011	16	64,000
100	8	128,000

Equation 9 shows the scaled Z-domain transfer function of the sinc filter.

$$H(Z) = \left[\frac{1 - Z^{-N}}{N(1 - Z^{-1})} \right]^5 \quad (9)$$

where

- N = decimation ratio

Equation 10 shows the frequency domain transfer function of the sinc filter.

$$|H(f)| = \left| \frac{\sin\left(\frac{\pi N \times f}{f_{MOD}} \right)}{N \sin\left(\frac{\pi \times f}{f_{MOD}} \right)} \right|^5 \quad (10)$$

where

- N = decimation ratio (see Table 7)

The sinc filter has notches (or zeros) that occur at the output data rate and multiples thereof. At these frequencies, the filter has zero gain. Figure 36 shows the frequency response of the sinc filter and Figure 37 shows the roll-off of the sinc filter.

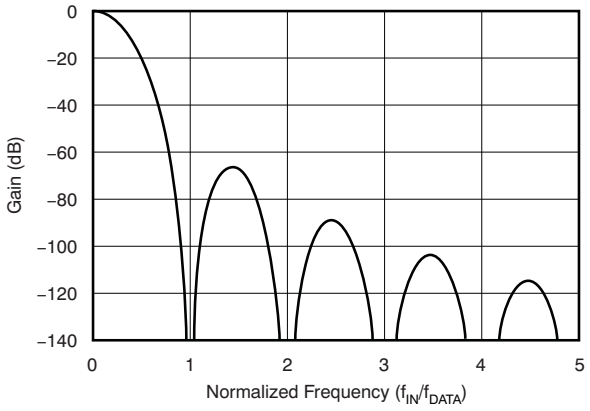


Figure 36. Sinc Filter Frequency Response (N = 32)

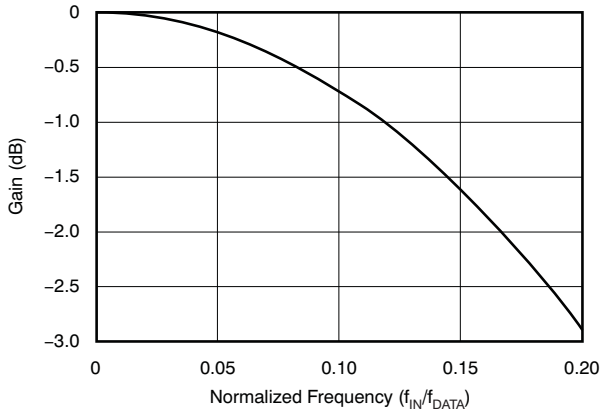


Figure 37. Sinc Filter Roll-Off

8.3.3.2.2 FIR Stage

The second stage of the ADS1283 digital filter is an FIR low-pass filter. Data are supplied to this stage from the sinc filter. The FIR stage is segmented into four substages, as shown in Figure 38.

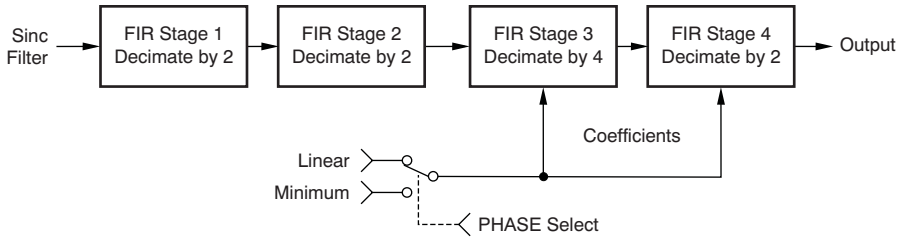


Figure 38. FIR Filter Substages

The first two substages are half-band filters with decimation ratios of two. The third substage decimates by four, and the fourth substage decimates by two. The overall decimation of the FIR stage is 32. Note that two coefficient sets are used for the third and fourth sections, depending on the phase selection. Table 8 lists the data rates and overall decimation ratio of the FIR stage. See Table 9 for the FIR filter coefficients.

Table 8. FIR Filter Data Rates

DR[2:0] REGISTER	DECIMATION RATIO (N)	FIR DATA RATE (SPS)
000	4096	250
001	2048	500
010	1024	1000
011	512	2000
100	256	4000

Table 9. FIR Stage Coefficients

COEFFICIENT	SECTION 1	SECTION 2	SECTION 3		SECTION 4	
	LINEAR PHASE SCALING = 1 / 512	LINEAR PHASE SCALING = 1 / 8388608	SCALING = 1 / 134217728		SCALING = 1 / 134217728	
			LINEAR PHASE	MINIMUM PHASE	LINEAR PHASE	MINIMUM PHASE
b_0	3	–10944	0	819	–132	11767
b_1	0	0	0	8211	–432	133882
b_2	–25	103807	–73	44880	–75	769961
b_3	0	0	–874	174712	2481	2940447
b_4	150	–507903	–4648	536821	6692	8262605
b_5	256	0	–16147	1372637	7419	17902757
b_6	150	2512192	–41280	3012996	–266	30428735
b_7	0	4194304	–80934	5788605	–10663	40215494
b_8	–25	2512192	–120064	9852286	–8280	39260213
b_9	0	0	–118690	14957445	10620	23325925
b_{10}	3	–507903	–18203	20301435	22008	–1757787
b_{11}		0	224751	24569234	348	–21028126
b_{12}		103807	580196	26260385	–34123	–21293602
b_{13}		0	893263	24247577	–25549	–3886901
b_{14}		–10944	891396	18356231	33460	14396783
b_{15}			293598	9668991	61387	16314388
b_{16}			–987253	327749	–7546	1518875
b_{17}			–2635779	–7171917	–94192	–12979500
b_{18}			–3860322	–10926627	–50629	–11506007
b_{19}			–3572512	–10379094	101135	2769794

Table 9. FIR Stage Coefficients (continued)

COEFFICIENT	SECTION 1	SECTION 2	SECTION 3		SECTION 4	
	LINEAR PHASE SCALING = 1 / 512	LINEAR PHASE SCALING = 1 / 8388608	SCALING = 1 / 134217728		SCALING = 1 / 134217728	
			LINEAR PHASE	MINIMUM PHASE	LINEAR PHASE	MINIMUM PHASE
b_{20}			–822573	–6505618	134826	12195551
b_{21}			4669054	–1333678	–56626	6103823
b_{22}			12153698	2972773	–220104	–6709466
b_{23}			19911100	5006366	–56082	–9882714
b_{24}			25779390	4566808	263758	–353347
b_{25}			27966862	2505652	231231	8629331
b_{26}			25779390	126331	–215231	5597927
b_{27}			19911100	–1496514	–430178	–4389168
b_{28}			12153698	–1933830	34715	–7594158
b_{29}			4669054	–1410695	580424	–428064
b_{30}			–822573	–502731	283878	6566217
b_{31}			–3572512	245330	–588382	4024593
b_{32}			–3860322	565174	–693209	–3679749
b_{33}			–2635779	492084	366118	–5572954
b_{34}			–987253	231656	1084786	332589
b_{35}			293598	–9196	132893	5136333
b_{36}			891396	–125456	–1300087	2351253
b_{37}			893263	–122207	–878642	–3357202
b_{38}			580196	–61813	1162189	–3767666
b_{39}			224751	–4445	1741565	1087392
b_{40}			–18203	22484	–522533	3847821
b_{41}			–118690	22245	–2490395	919792
b_{42}			–120064	10775	–688945	–2918303
b_{43}			–80934	940	2811738	–2193542
b_{44}			–41280	–2953	2425494	1493873
b_{45}			–16147	–2599	–2338095	2595051
b_{46}			–4648	–1052	–4511116	–79991
b_{47}			–874	–43	641555	–2260106
b_{48}			–73	214	6661730	–963855
b_{49}			0	132	2950811	1482337
b_{50}			0	33	–8538057	1480417
b_{51}			0	0	–10537298	–586408
b_{52}					9818477	–1497356
b_{53}					41426374	–168417
b_{54}					56835776	1166800
b_{55}					41426374	644405
b_{56}					9818477	–675082
b_{57}					–10537298	–806095
b_{58}					–8538057	211391
b_{59}					2950811	740896
b_{60}					6661730	141976
b_{61}					641555	–527673
b_{62}					–4511116	–327618
b_{63}					–2338095	278227
b_{64}					2425494	363809

Table 9. FIR Stage Coefficients (continued)

COEFFICIENT	SECTION 1	SECTION 2	SECTION 3		SECTION 4	
	LINEAR PHASE SCALING = 1 / 512	LINEAR PHASE SCALING = 1 / 8388608	SCALING = 1 / 134217728		SCALING = 1 / 134217728	
			LINEAR PHASE	MINIMUM PHASE	LINEAR PHASE	MINIMUM PHASE
b_{65}					2811738	–70646
b_{66}					–688945	–304819
b_{67}					–2490395	–63159
b_{68}					–522533	205798
b_{69}					1741565	124363
b_{70}					1162189	–107173
b_{71}					–878642	–131357
b_{72}					–1300087	31104
b_{73}					132893	107182
b_{74}					1084786	15644
b_{75}					366118	–71728
b_{76}					–693209	–36319
b_{77}					–588382	38331
b_{78}					283878	38783
b_{79}					580424	–13557
b_{80}					34715	–31453
b_{81}					–430178	–1230
b_{82}					–215231	20983
b_{83}					231231	7729
b_{84}					263758	–11463
b_{85}					–56082	–8791
b_{86}					–220104	4659
b_{87}					–56626	7126
b_{88}					134826	–732
b_{89}					101135	–4687
b_{90}					–50629	–976
b_{91}					–94192	2551
b_{92}					–7546	1339
b_{93}					61387	–1103
b_{94}					33460	–1085
b_{95}					–25549	314
b_{96}					–34123	681
b_{97}					348	16
b_{98}					22008	–349
b_{99}					10620	–96
b_{100}					–8280	144
b_{101}					–10663	78
b_{102}					–266	–46
b_{103}					7419	–42
b_{104}					6692	9
b_{105}					2481	16
b_{106}					–75	0
b_{107}					–432	–4
b_{108}					–132	0
b_{109}					0	0

As shown in Figure 39, the FIR frequency response provides a flat pass band to 0.375 of the data rate (±0.003 dB pass-band ripple). Figure 40 shows the transition from pass band to stop band.

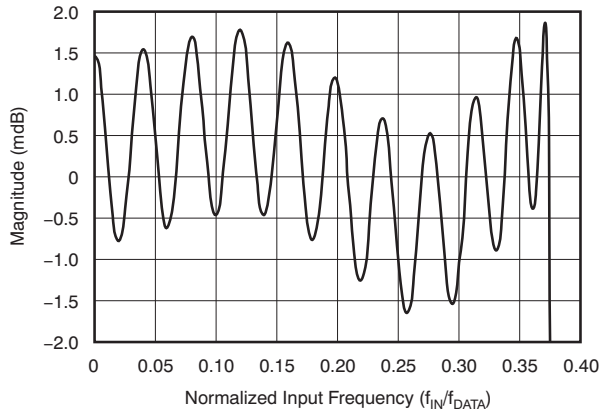


Figure 39. FIR Pass-Band Magnitude Response (f_{DATA} = 500 Hz)

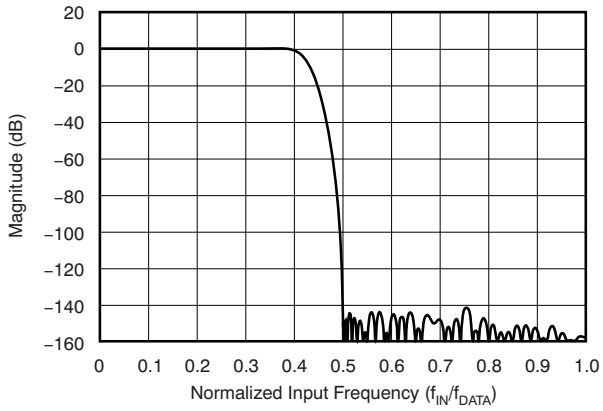


Figure 40. FIR Transition Band Magnitude Response

Although not shown in Figure 40, the pass-band response repeats at multiples of the modulator frequency ($Nf_{MOD} – f_0$ and $Nf_{MOD} + f_0$, where N = 1, 2, and so on, and f_0 = pass band). These image frequencies, if present in the signal and not externally filtered, fold back (or alias) into the pass band and cause errors. A low-pass signal filter reduces the effect of aliasing. Often, the RC low-pass filter provided by the PGA output resistors and the external capacitor connected to CAPP and CAPN provide sufficient signal attenuation.

8.3.3.2.3 Group Delay and Step Response

The FIR block is implemented as a multistage FIR structure with selectable linear or minimum phase response. The pass band, transition band, and stop band responses of the filters are nearly identical but differ in the respective phase responses.

8.3.3.2.3.1 Linear Phase Response

Linear phase filters exhibit constant delay time versus input frequency (that is, constant group delay). Linear phase filters have the property that the time delay is constant from any instant of the input signal to the same instant of the output data, and is independent of the signal nature. This filter behavior results in essentially zero phase error when analyzing multitone signals. However, the group delay and settling time of the linear phase filter are somewhat larger than the minimum phase filter, as shown in Figure 41.

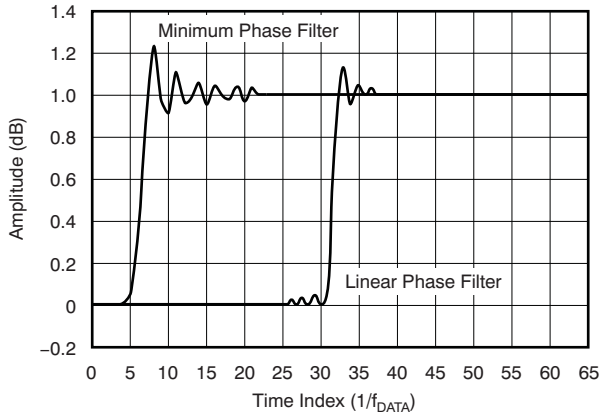


Figure 41. FIR Step Response

8.3.3.2.3.2 Minimum Phase Response

The minimum phase filter provides a short delay from the arrival of an input signal to the output, but the relationship (phase) is not constant versus frequency, as shown in Figure 42. The filter phase is selected by the PHS bit, as Table 10 shows.

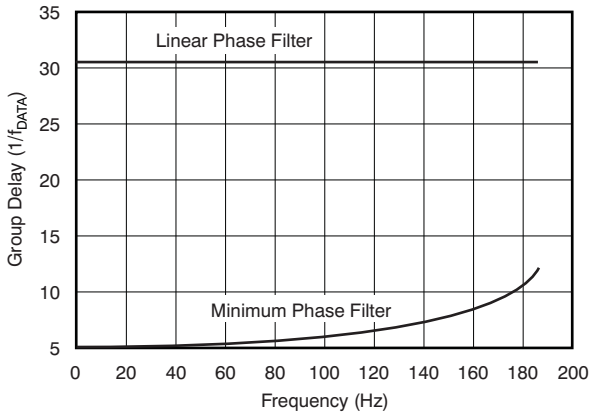


Figure 42. FIR Group Delay (f_{DATA} = 500Hz)

Table 10. FIR Phase Selection

PHS BIT	FILTER PHASE
0	Linear
1	Minimum

8.3.3.2.4 HPF Stage

The last stage of the ADS1283 filter block is a first-order HPF implemented as an IIR structure. This filter stage blocks dc signals, and rolls off low-frequency components below the cutoff frequency. The transfer function for the filter is shown in Equation 11:

$$HPF(Z) = \frac{2 - a}{2} \times \frac{1 - Z^{-1}}{1 - bZ^{-1}} \quad (11)$$

where

- *b* is calculated as shown in Equation 12

$$b = \frac{1 + (1 - a)^2}{2} \quad (12)$$

The high-pass corner frequency is programmed by registers HPF[1:0], in hexadecimal. Equation 13 is used to set the high-pass corner frequency. Table 11 lists example values for the high-pass filter.

$$HPF[1:0] = 65{,}536 \left[1 - \sqrt{1 - 2\frac{\cos \omega_N + \sin \omega_N - 1}{\cos \omega_N}} \right] \quad (13)$$

where

- HPF = High-pass filter register value (converted to hexadecimal)
- $\omega_N = 2\pi f_{HP} / f_{DATA}$ (normalized frequency, radians)
- f_{HP} = High-pass corner frequency (Hz)
- f_{DATA} = Data rate (Hz)

Table 11. High-Pass Filter Value Examples

f_{HP} (Hz)	DATA RATE (SPS)	HPF[1:0]
0.5	250	0337h
1.0	500	0337h
1.0	1000	019Ah

The HPF causes a small gain error, in which case the magnitude of the error depends on the ratio of f_{HP} / f_{DATA}. For many common values of (f_{HP} / f_{DATA}), the gain error is negligible. Figure 43 shows the gain error of the HPF.

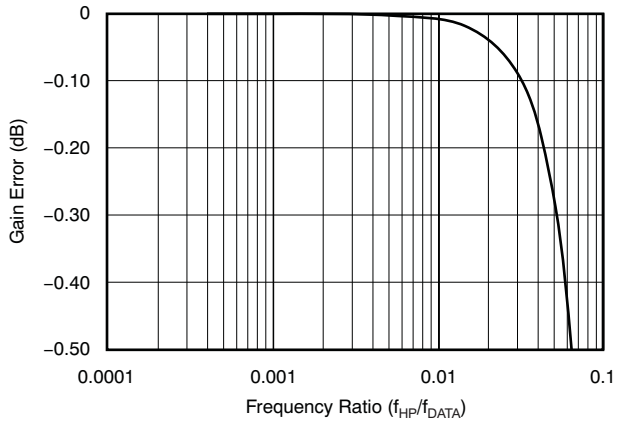


Figure 43. HPF Gain Error

The gain error factor is illustrated in Equation 14:

$$\text{HPF Gain} = \frac{1 + \sqrt{1 - 2\left(\frac{\cos\omega_N + \sin\omega_N - 1}{\cos\omega_N}\right)}}{2 - \left(\frac{\cos\omega_N + \sin\omega_N - 1}{\cos\omega_N}\right)} \quad (14)$$

Figure 44 shows the first-order amplitude and phase response of the HPF. In the case of applying step inputs or synchronizing, make sure to take the settling time of the filter into account.

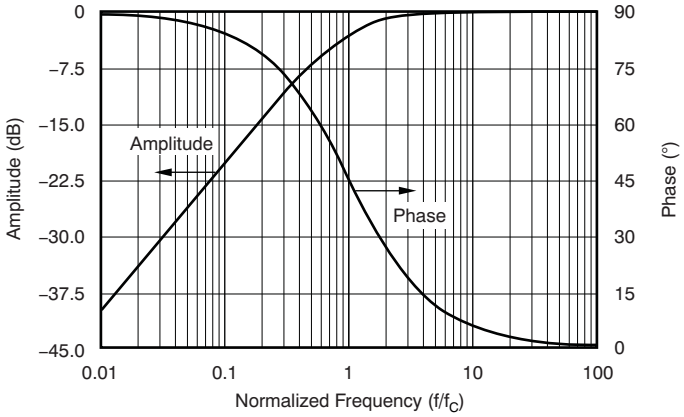


Figure 44. HPF Amplitude and Phase Response

8.3.4 Master Clock Input (CLK)

The ADS1283 requires a clock for operation. The nominal clock frequency is 4.096 MHz. The clock is applied to the CLK pin. The ADC data rates scale with CLK frequency, however there is no benefit in noise by reducing the CLK frequency.

As with any high-speed data converter, a high-quality, low-jitter clock is essential for optimum performance. Crystal clock oscillators are the recommended clock source. Make sure to avoid excess ringing on the clock input; keep the clock trace as short as possible and use a 50-Ω series resistor close to the source.

8.4 Device Functional Modes

8.4.1 Synchronization (SYNC PIN and SYNC Command)

The ADS1283 can be synchronized to an external event, as well as to other ADS1283 devices if the synchronization is applied simultaneously.

The ADS1283 has two sources for synchronization: the SYNC input pin and the SYNC command. The ADS1283 also has two synchronizing modes: *pulse-sync* and *continuous-sync*. In pulse-sync mode, the ADS1283 synchronizes to a single synchronization. In continuous-sync mode, either a single synchronization is used to synchronize conversions, or a continuous clock is applied to the pin with a period equal to integer multiples of the data rate. When the periods of the SYNC input and the $\overline{\text{DRDY}}$ output do not match, the ADS1283 resynchronizes and conversions are restarted.

8.4.1.1 Pulse-Sync Mode

In pulse-sync mode, when a synchronization occurs (by pin or command), the ADS1283 unconditionally stops and restarts the conversion process. When the ADC synchronizes, the device resets the internal filter memory, $\overline{\text{DRDY}}$ goes high, and after the digital filter has settled, new conversion data are available as shown in Figure 45 and Table 12.

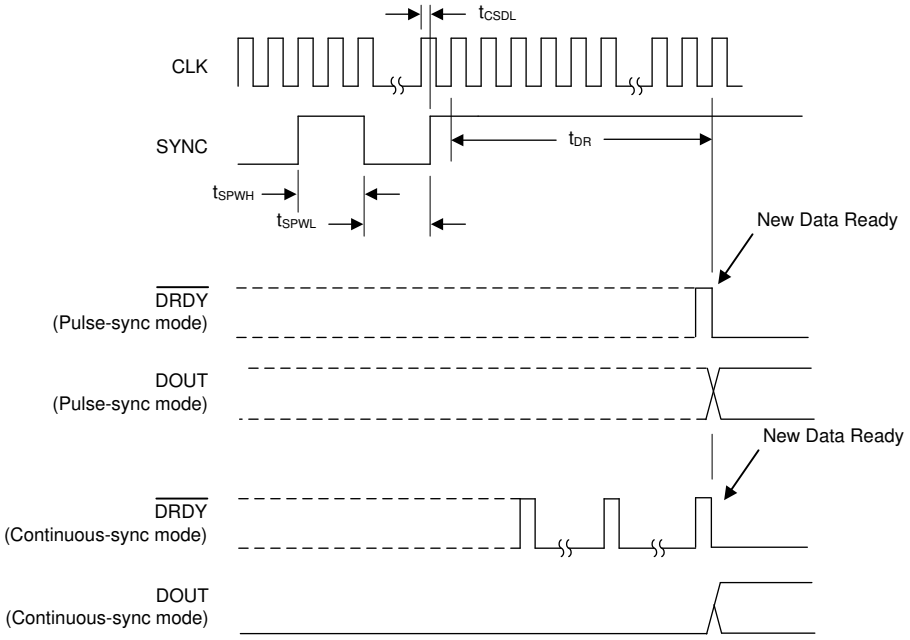


Figure 45. Pulse-Sync and Continuous-Sync Timing With Single Synchronization

Table 12. Pulse-Sync Timing for Figure 45 and Figure 46

PARAMETER		MIN	MAX	UNIT
t_{CSDL}	CLK rising edge to SYNC rising edge (1)	30	–30	ns
t_{SYNC}	SYNC clock period (2)	1	Infinite	n / f_{DATA}
$t_{SPWH, L}$	SYNC pulse width, high or low	2		1 / f_{CLK}
t_{DR}	Time for data ready (SINC filter)	See Table 13		
	Time for data ready (FIR filter)	62.98046875 / f_{DATA} + 468 / f_{CLK}		

(1) CLK rising edge to SYNC rising edge timing must not occur within the specified time window.
(2) Continuous-sync mode; a free-running clock applied to the SYNC input without causing resynchronization. See Figure 46

Table 13. t_{DR} Time for Data Ready (Sinc Filter)

f_{DATA} (kSPS)	f_{CLK} CYCLES(1)
128	440
64	616
32	968
16	1672
8	2824

(1) For SYNC and WAKEUP commands, number of f_{CLK} cycles from next rising CLK edge directly after eighth rising SCLK edge to $\overline{DRDY}$ falling edge. For WAKEUP command only, subtract two f_{CLK} cycles.

Table 13 is referenced by Table 12 and Table 15.

Observe the timing restriction of SYNC rising edge to CLK rising edge as shown in Figure 45 and Table 12. Synchronization occurs on the next rising CLK edge after the rising edge of the SYNC, or after the eighth rising SCLK edge when synchronized by command. To synchronize multiple ADCs, broadcast the command to the ADCs simultaneously.

8.4.1.2 Continuous-Sync Mode

In continuous-sync mode, either a single synchronization pulse or a continuous clock may be applied. When a single synchronization pulse is applied (rising edge), the device resynchronizes as it does in pulse-sync mode. ADC resynchronization occurs only under the condition that the time from the previous rising edge of SYNC is not a multiple of the conversion period. When resynchronization occurs in continuous-sync mode, $\overline{DRDY}$ continues to toggle unaffected, and the DOUT output is held low until data are ready (63 $\overline{DRDY}$ periods later). At the 63rd reading, conversion data are valid (when the conversion data are non-zero), as shown in Figure 45.

When a continuous clock is applied to the SYNC pin, the period must be an integral multiple of the output data rate or the device resynchronizes. Note that synchronization results in the restarting of the digital filter and an interruption of 63 readings (as shown in Table 12).

If a SYNC clock is applied to the ADC, the device resynchronizes only under the condition $t_{SYNC} \neq N / f_{DATA}$, where N = 1, 2, 3, and so on. $\overline{DRDY}$ continues to output, but DOUT is held low until the new data are ready. If a SYNC clock is applied and the clock period matches an integral multiple of the output data rate, the device freely runs without resynchronization. Note that the phase of the applied clock and output data rate ($\overline{DRDY}$) are not aligned because of the initial delay of $\overline{DRDY}$ after the SYNC clock is first applied. Figure 46 shows the timing for continuous-sync mode.

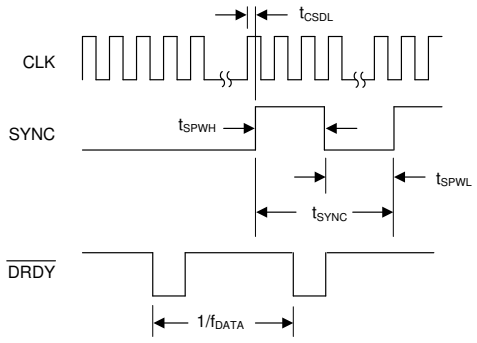


Figure 46. Continuous-Sync Timing With SYNC Clock

Apply a SYNC clock input after the continuous-sync mode is set. The first rising edge of SYNC then causes a synchronization. Note that subsequent writes to any ADC register results in resynchronization at the time of the register write operation. The resynchronization leads to loss of the SYNC-pin controlled synchronization performed previously. Send the STANDBY command followed by the WAKEUP command to reestablish the SYNC-pin synchronization. Resynchronization to the SYNC pin occurs as long as the time between the STANDBY and WAKEUP commands is not a multiple integer of the conversion period by at least one clock cycle.

8.4.2 Reset ($\overline{\text{RESET}}$ Pin and Reset Command)

The ADS1283 can be reset in two ways: toggle the $\overline{\text{RESET}}$ pin low, or send a RESET command. When using the $\overline{\text{RESET}}$ pin, take it low and hold for at least 2 / f_{CLK} to force a reset. The ADS1283 is held in reset until the pin is released. By command, reset takes effect on the next rising edge of f_{CLK} after the eighth rising edge of SCLK of the command. In order to make certain that the RESET command can function, the SPI interface may need to be reset; see the *Serial Interface* section.

When the ADS1283 is reset, registers are set to default and the conversions are synchronized on the next rising edge of CLK. New conversion data are available, as shown in Figure 47 and Table 14.

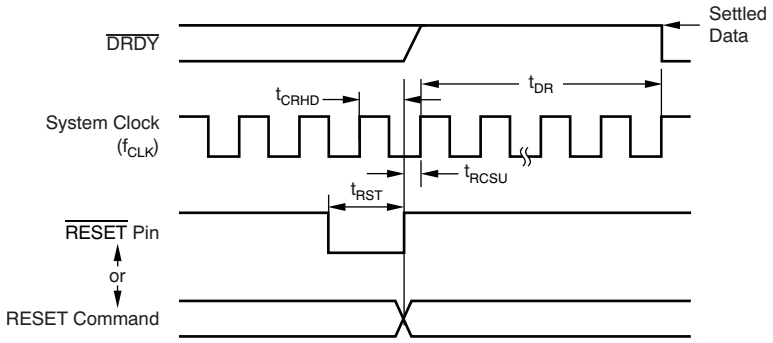


Figure 47. Reset Timing

Table 14. Reset Timing for Figure 47

PARAMETER		MIN	UNIT
t_{CRHD}	CLK to RESET hold time	10	ns
t_{RCSU}	RESET to CLK setup time	10	ns
t_{RST}	RESET low	2	1 / f_{CLK}
t_{DR}	Time for data ready	62.98046875 / f_{DATA} + 468 / f_{CLK}	s

8.4.3 Power-Down ($\overline{\text{PWDN}}$ Pin and STANDBY Command)

There are two ways to power-down the ADS1283: take the $\overline{\text{PWDN}}$ pin low, or send a STANDBY command. When the $\overline{\text{PWDN}}$ pin is pulled low, the internal circuitry is disabled to minimize power and the contents of the register settings are reset.

When in a power-down state, the device outputs remain active and the device inputs must not float. When the STANDBY command is sent, the SPI port and the configuration registers are kept active. Figure 48 and Table 15 show the timing. Standby mode is cancelled when $\overline{\text{CS}}$ is taken high.

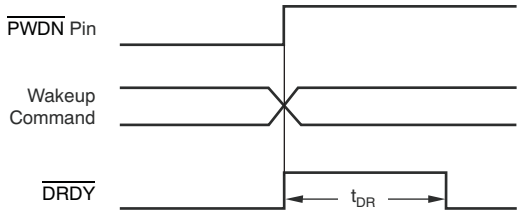


Figure 48. $\overline{\text{PWDN}}$ Pin and Wake-Up Command Timing (t_{DR} shows Table 15)

Table 15. Power-On, $\overline{\text{PWDN}}$ Pin, and Wake-Up Command Timing for New Data

PARAMETER			FILTER MODE
t_{DR}	Time for data ready 2^{16} CLK cycles after power-on; and new data ready after $\overline{\text{PWDN}}$ pin or WAKEUP command	See Table 13	SINC(1)
		62.98046875 / f_{DATA} + 468 / f_{CLK} (2)	FIR

(1) Supply power-on and $\overline{\text{PWDN}}$ pin default is 1000 SPS FIR.
(2) Subtract two CLK cycles for the WAKEUP command. The WAKEUP command is timed from the next rising edge of CLK to after the eighth rising edge of SCLK during command to $\overline{\text{DRDY}}$ falling.

8.4.4 Power-On Sequence

The ADS1283 has three power supplies: AVDD, AVSS, and DVDD. Figure 49 shows the power-on sequence of the ADS1283. The power supplies can be sequenced in any order. The supplies [the difference of (AVDD – AVSS) and DVDD] generate signals that are ANDed together for the internal reset. After the supplies have crossed the minimum thresholds, 2^{16} f_{CLK} cycles are counted before releasing the internal reset. After the internal reset is released, new conversion data are available, as shown in Figure 49 and Table 15.

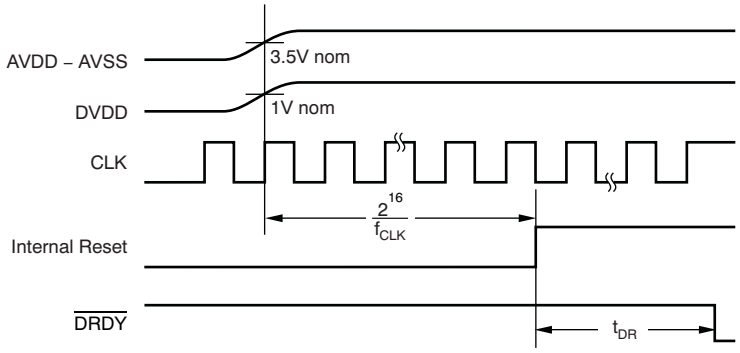


Figure 49. Power-On Sequence

8.4.5 DVDD Power Supply

The DVDD supply operates over the range of 1.65 V to 3.6 V. If operating DVDD at less than 2.25 V, connect the DVDD pin to the BYPAS pin. Otherwise, do not connect these pins together. Figure 50 shows this connection.

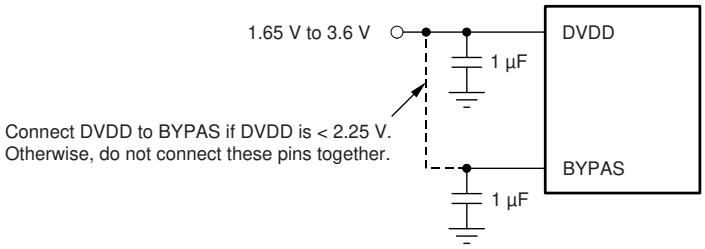


Figure 50. DVDD Power

8.4.6 Serial Interface

A serial interface is used to read both the conversion data and to access the configuration registers. The interface is SPI-compatible and consists of four signals: $\overline{CS}$, SCLK, DIN, and DOUT. A minimum of 16 ADCs converting at 4 kSPS can share a common serial bus when operating SCLK at 2 MHz.

8.4.6.1 Chip Select ($\overline{CS}$)

Chip select ($\overline{CS}$) is an active-low input that enables the ADC serial interface for data transfer. When $\overline{CS}$ is low, the serial interface is enabled for communication. When $\overline{CS}$ is high, the serial interface is disabled. When the serial interface is disabled, the DOUT (output data pin) is high impedance (tristate or Hi-Z). When $\overline{CS}$ is high, SCLK activity is ignored, and data transfers or commands in progress are reset. $\overline{CS}$ must remain low for the duration of the data transfer with the ADC. $\overline{CS}$ can be tied low, which permanently enables the ADC serial interface. When $\overline{CS}$ goes high, the ADC idles (STANDBY) and stop read data continuous (SDATAC) modes are cancelled. See the *SDATAC Requirements* section for more information about SDATAC mode.

8.4.6.2 Serial Clock (SCLK)

The serial clock (SCLK) is an input pin that is used to clock data into (DIN) and out of (DOUT) the ADC. SCLK is a Schmitt-trigger input that has a high degree of noise immunity. However, keep SCLK as clean as possible to prevent possible glitches from inadvertently shifting the data.

Data are shifted into DIN on the rising edge of SCLK and data are shifted out of DOUT on the falling edge of SCLK. Keep SCLK low when not active. SCLK is ignored when $\overline{CS}$ is high.

8.4.6.3 Data Input (DIN)

The data input pin (DIN) is used to input register data and commands to the ADS1283. Keep DIN low when reading conversion data in the read-data-continuous mode (except when issuing a SDATAC command). Data on DIN are shifted into the converter on the rising edge of SCLK.

8.4.6.4 Data Output (DOUT)

The data output pin (DOUT) is used to output data from the ADS1283. Data are shifted out on the falling edge of SCLK. When $\overline{CS}$ is high, the DOUT pin is in tristate.

8.4.6.5 Serial Port Auto Timeout

The serial interface is reset each time $\overline{CS}$ is taken high. However, for applications that tie $\overline{CS}$ low, the serial port cannot be reset by taking $\overline{CS}$ high; reset of the serial interface is no longer possible by using $\overline{CS}$. The ADS1283 provides a feature that automatically recovers the interface when a transmission is stopped or interrupted, or if an inadvertent glitch appears on SCLK. To reset the serial interface, hold SCLK low for 64 $\overline{DRDY}$ cycles. The reset of the serial interface results in termination of data transfer or commands in progress. After serial port reset occurs, the next SCLK pulse starts a new communication cycle. To prevent automatic reset from occurring, pulse SCLK at least once for every 64 DRDY pulses.

8.4.6.6 Data Ready ($\overline{DRDY}$)

$\overline{DRDY}$ is an output that is driven low when new conversion data are ready, as shown in Figure 51. When reading data in continuous mode, the read operation must be completed before four CLK periods before the next falling $\overline{DRDY}$ goes low again, or the data are overwritten with new conversion data. When reading data in command mode, the read operation can overlap the occurrence of the next $\overline{DRDY}$ without data corruption.

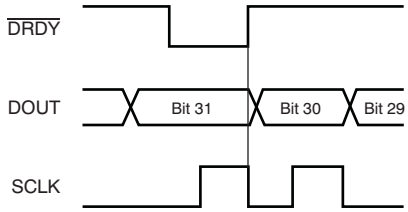


Figure 51. $\overline{DRDY}$ With Data Retrieval

$\overline{DRDY}$ resets high on the first falling edge of SCLK. Figure 51 and Figure 52 show the function of $\overline{DRDY}$ with and without data readback, respectively.

If data are not retrieved (no SCLK provided), $\overline{DRDY}$ pulses high for four f_{CLK} periods during the update time, as shown in Figure 52.

$\overline{DRDY}$ remains active when $\overline{CS}$ is high.

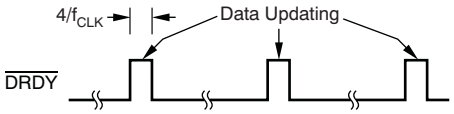


Figure 52. $\overline{DRDY}$ With No Data Retrieval

8.4.7 Data Format

The ADS1283 output data is 32-bits in binary twos complement format, as shown in Table 16. The LSB of the data is a redundant sign bit: 0 for positive numbers and 1 for negative numbers. However, when the output is clipped to +FS, the LSB = 1, and when the output is clipped to –FS, the LSB = 0. If desired, the data readback can be stopped at 24 bits. Note that in sinc-filter mode, the output data are scaled by ½.

Table 16. Ideal Output Code Versus Input Signal

INPUT SIGNAL V_{IN} (AINP – AINN)	32-BIT IDEAL OUTPUT CODE(1)	
	FIR FILTER	SINC FILTER(2)
$> \frac{V_{REF}}{2 \times PGA}$	7FFFFFFFh	See note (3)
$\frac{V_{REF}}{2 \times PGA}$	7FFFFFFEh	3FFFFFFFh
$\frac{V_{REF}}{2PGA \times (2^{30} - 1)}$	00000002h	00000001h
0	00000000h	00000000h
$\frac{-V_{REF}}{2PGA \times (2^{30} - 1)}$	FFFFFFFFh	FFFFFFFFh
$\frac{-V_{REF}}{2PGA} \times \frac{2^{30}}{2^{30} - 1}$	80000001h	C0000000h
$< \frac{-V_{REF}}{2PGA} \times \frac{2^{30}}{2^{30} - 1}$	80000000h	See note (3)

(1) Excludes effects of noise, linearity, offset, and gain errors.
(2) Due to the reduction in oversampling ratio (OSR) related to high data rates of the sinc filter, full resolution may not be available.
(3) In sinc-filter mode, the output does not clip at half-scale code when the full-scale range is exceeded.

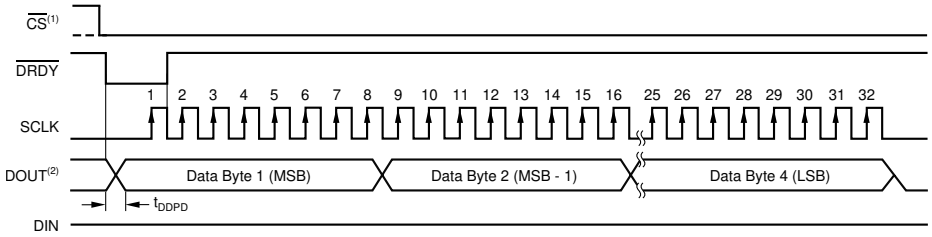
8.4.8 Reading Data

The ADS1283 provides two modes to read conversion data: read-data-continuous and read-data-by-command.

8.4.8.1 Read-Data-Continuous Mode

In the read-data-continuous mode, the conversion data are shifted out directly from the device without the need for sending a read command. This mode is the default mode at power-on. This mode is also enabled by the RDATAC command. When $\overline{DRDY}$ goes low, indicating that new data are available, the MSB of data appears on DOUT, as shown in Figure 53. The data are normally read on the rising edge of SCLK, at the occurrence of the first falling edge of SCLK, $\overline{DRDY}$ returns high. After 32 bits of data have been shifted out, further SCLK transitions cause DOUT to go low. If desired, the read operation may be stopped at 24 bits. The data shift operation must be completed within four CLK periods before $\overline{DRDY}$ falls again or the data may be corrupted.

When a SDATAC command is issued, the $\overline{DRDY}$ output is blocked but the ADS1283 continues conversions. In stop continuous mode, the data can only be read by command.



(1) DOUT is in tristate when $\overline{CS}$ is high. $\overline{CS}$ can be tied low. See Figure 1 for $\overline{CS}$ low to valid DOUT propagation time.

Figure 53. Read Data Continuous

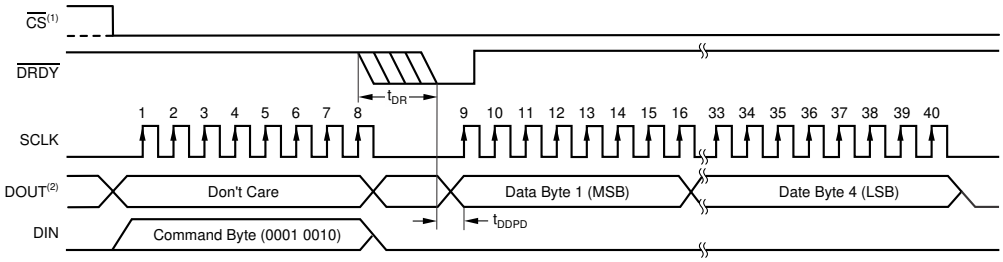
Table 17. Timing Data for Figure 53

PARAMETER		MIN	TYP	MAX	UNIT
t_{DDPD}	$\overline{DRDY}$ to valid MSB on DOUT propagation delay(1)			100	ns

(1) DOUT is in tristate when $\overline{CS}$ is high. Load on DOUT = 20 pF || 100 kΩ.

8.4.8.2 Read-Data-By-Command Mode

Read-data-continuous mode is stopped by the SDATAC command and put into read-data-by-command mode. In read-data-by-command mode, an RDATA command must be sent to the device for each data conversion (as shown in Figure 54). When the read data command is received (on the eighth SCLK rising edge), data are available to read only when $\overline{DRDY}$ goes low (t_{DR}). When $\overline{DRDY}$ goes low, conversion data appear on DOUT. The data may be read on the rising edge of SCLK.



(1) DOUT is in tristate when $\overline{CS}$ is high.$\overline{CS}$ can be tied low. See Figure 1 for $\overline{CS}$ low to SCLK rising edge time.

Figure 54. Read Data By Command, RDATA (t_{DDPD} timing is given in Table 17)

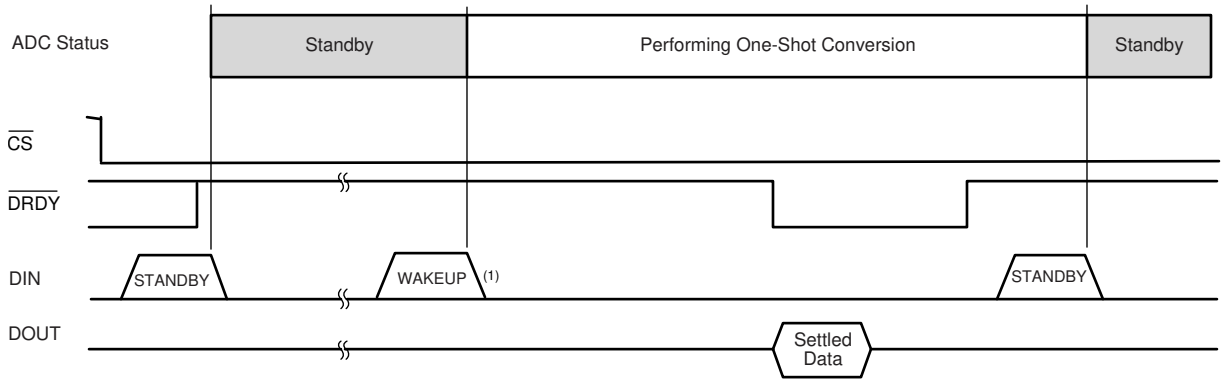
Table 18. Read Data Timing for Figure 54

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{DR}	Time for new data after data read command	0		1	f_{DATA}

8.4.9 One-Shot Operation

The ADS1283 can perform very power-efficient, one-shot conversions using the STANDBY command while under software control. Figure 55 shows this sequence. First, issue the STANDBY command to set the standby mode.

When ready to make a measurement, issue the WAKEUP command. When $\overline{\text{DRDY}}$ goes low, the fully-settled conversion data are ready and can be read directly in read-data-continuous mode. Afterwards, issue another STANDBY command. When ready for the next measurement, repeat the cycle starting with another WAKEUP command.



See Figure 48 and Table 15 for time to new data.

Figure 55. One-Shot Conversions Using the STANDBY Command

8.4.10 Offset and Full-Scale Calibration Registers

The conversion data can be scaled for offset and gain before yielding the final output code. As shown in Figure 56, the output of the digital filter is first subtracted by the offset register (OFC) and then multiplied by the full-scale register (FSC). Equation 15 shows the scaling:

$$\text{Final Output Data} = (\text{Input} - \text{OFC}[2:0]) \times \frac{\text{FSC}[2:0]}{400000\text{h}} \tag{15}$$

The values of the offset and full-scale registers are set by writing to them directly, or they are set automatically by the calibration commands.

The offset and full-scale calibrations apply to specific PGA settings. When the PGA is changed, these registers generally require recalculation. Calibration is bypassed in the sinc filter mode.

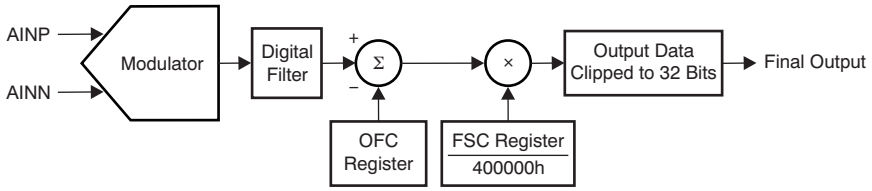


Figure 56. Calibration Block Diagram

8.4.10.1 OFC[2:0] Registers

The 24-bit offset calibration word is composed of three 8-bit registers, as shown in Table 19. The offset register is left-justified to align with the 32 bits of conversion data. The offset is in twos complement format with a maximum positive value of 7FFFFFh and a maximum negative value of 800000h. This value is subtracted from the conversion data. A register value of 00000h has no offset correction (default value).

Table 19. Offset Calibration Word

REGISTER	BYTE	BIT ORDER							
OFC0	LSB	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
OFC1	MID	B15	B14	B13	B12	B11	B10	B9	B8
OFC2	MSB	B23 (MSB)	B22	B21	B20	B19	B18	B17	B16

Although the offset calibration register value can correct offsets ranging from –FS to +FS (as shown in Table 20), in order to avoid input overload, do not exceed the maximum input voltage range of 106% FSR (including calibration).

Table 20. Offset Calibration Values

OFC REGISTER	FINAL OUTPUT CODE(1)
7FFFFFh	80000000h
000001h	FFFFFF00h
000000h	00000000h
FFFFFFh	00000100h
800000h	7FFFFF00h

(1) Full 32-bit final output code with zero code input.

8.4.10.2 FSC[2:0] Registers

The full-scale calibration is a 24-bit word, composed of three 8-bit registers, as shown in Table 21. The full-scale calibration value is 24-bit, straight offset binary, normalized to 1.0 at code 400000h.

Table 21. Full-Scale Calibration Word

REGISTER	BYTE	BIT ORDER							
FSC0	LSB	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
FSC1	MID	B15	B14	B13	B12	B11	B10	B9	B8
FSC2	MSB	B23 (MSB)	B22	B21	B20	B19	B18	B17	B16

Table 22 summarizes the scaling of the full-scale register. A register value of 400000h (default value) has no gain correction (gain = 1). Although the full-scale calibration register value corrects gain errors above one (gain correction < 1), the full-scale range of the analog inputs must not exceed 106% FSR (including calibration) in order to avoid input overload.

Table 22. Full-Scale Calibration Register Values

FSC REGISTER	GAIN CORRECTION
800000h	2.0
400000h	1.0
200000h	0.5
000000h	0

8.4.11 Calibration Commands (OFSCAL and GANCAL)

Use the calibration commands (OFSCAL or GANCAL) to calibrate the conversion data. The values of the offset and gain calibration registers are internally written to perform calibration. The appropriate input signals must be applied to the ADS1283 inputs before sending the commands. Use slower data rates to achieve more consistent calibration results; this effect is a byproduct of the lower noise that these data rates provide. Also, if calibrating at power-on, be sure the reference voltage is fully settled.

Figure 57 shows the calibration command sequence. After the analog input voltage (and reference) have stabilized, send the SDATAC command, followed by the SYNC and RDATAC commands. DRDY goes low after 64 data periods. After DRDY goes low, send the SDATAC command, then the calibrate command (OFSCAL or GANCAL), followed by the RDATAC command. After 16 data periods, calibration is complete and conversion data can be read at this time. The SYNC input must remain high during the calibration sequence.

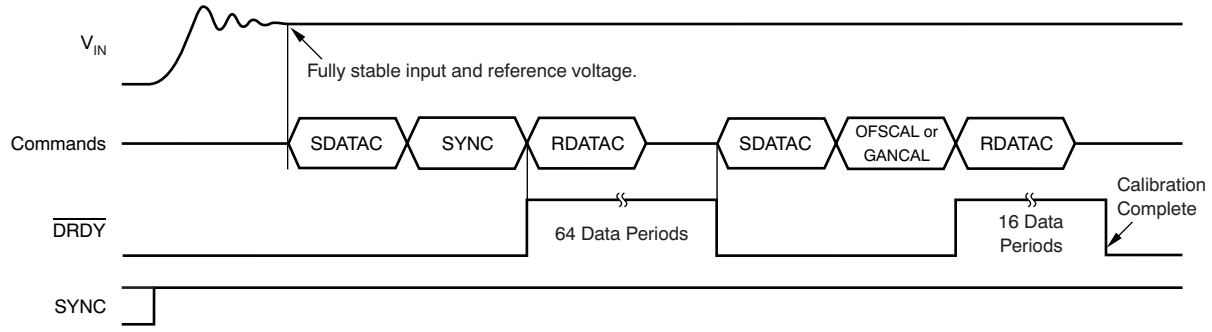


Figure 57. Offset and Gain Calibration Timing

The calibration commands apply to specific PGA settings. If the PGA is changed, recalibration is necessary. Calibration is bypassed in the sinc filter mode.

8.4.11.1 OFSCAL Command

The OFSCAL command performs an offset calibration. Before sending the OFSCAL command sequence (Figure 57), a *zero* input signal must be applied to the ADS1283 and the inputs allowed to stabilize. When the command sequence (Figure 57) is sent, the ADS1283 averages 16 readings, and then writes this value to the OFC register. The contents of the OFC register can be subsequently read or written. During offset calibration, the full-scale correction is bypassed. Use the OFSCAL command to calibrate the optional 100-mV offset.

8.4.11.2 GANCAL Command

The GANCAL command performs a gain calibration. Before sending the GANCAL command sequence (Figure 57), a dc input must be applied (typically full-scale input, but not to exceed 106% full-scale). After the signal has stabilized, the command sequence can be sent. The ADS1283 averages 16 readings, then computes a gain value that scales the applied calibration voltage to full-scale. The gain value is written to the FSC register, where the contents are subsequently read or written.

8.4.12 User Calibration

System calibration of the ADS1283 can be performed without using the calibration commands. This procedure requires the calibration values to be externally calculated and then written to the calibration registers. The steps for this procedure are:

1. Set the OFSCAL[2:0] register = 0h, and GANCAL[2:0] = 400000h. These values set the offset and gain registers to 0 and 1, respectively.
2. Apply a zero differential input to the input of the system. Wait for the system to settle and then average the output readings. Higher numbers of averaged readings result in more consistent calibration. Write the averaged value to the OFC register.
3. Apply a differential dc signal, or an ac signal (typically full-scale, but do not exceed 106% FSR). Wait for the system to settle and then average the output readings.

The value written to the FSC registers is calculated by Equation 16 or Equation 17.

DC-signal calibration is shown in Equation 16. The expected output code is based on 31-bit output data.

$$\text{FSC[2:0]} = 400000\text{h} \times \left(\frac{\text{Expected Output Code}}{\text{Actual Output Code}} \right) \tag{16}$$

For ac-signal calibration, use an RMS value of collected data, as shown in Equation 17:

$$\text{FSC[2:0]} = 400000\text{h} \times \frac{\text{Expected RMS Value}}{\text{Actual RMS Value}} \tag{17}$$

8.5 Programming

8.5.1 Commands

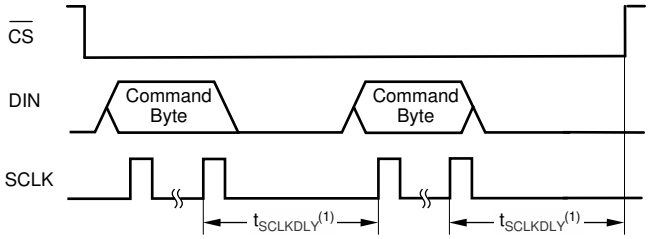
The commands listed in Table 23 control the operation of the ADS1283. Most commands are stand-alone (that is, one byte in length); the register read and write commands are two bytes long in addition to the actual register data bytes.

Table 23. Command Descriptions

COMMAND	TYPE	DESCRIPTION	1st COMMAND BYTE(1)(2)	2nd COMMAND BYTE(3)
WAKEUP	Control	Wake-up from standby mode	0000 000X (00h or 01h)	
STANDBY	Control	Enter standby mode	0000 001X (02h or 03h)	
SYNC	Control	Synchronize the analog-to-digital conversion	0000 010X (04h or 5h)	
RESET	Control	Reset registers to default values	0000 011X (06h or 07h)	
RDATAC	Control	Enter read data continuous mode	0001 0000 (10h)	
SDATAC	Control	Stop read data continuous mode	0001 0001 (11h)	
RDATA	Data	Read data by command(4)	0001 0010 (12h)	
RREG	Register	Read *nnnnn* register(s) at address *rrrrr*(4)	001*r rrrr* (20h + 000*r rrrr*)	000*n nnnn* (00h + *n nnnn*)
WREG	Register	Write *nnnnn* register(s) at address *rrrrr*	010*r rrrr* (40h + 000*r rrrr*)	000*n nnnn* (00h + *n nnnn*)
OFSCAL	Calibration	Offset calibration	0110 0000 (60h)	
GANCAL	Calibration	Gain calibration	0110 0001 (61h)	

(1) X = don't care.
(2) *rrrrr* = starting address for register read and write commands.
(3) *nnnnn* = number of registers to be read from or written to – 1. For example, to read from or write to three registers, set *nnnnn* = 2 (00010).
(4) Required to cancel read-data-continuous mode before sending a command.

$\overline{CS}$ must remain low for duration of the command-byte sequence. A delay of 24 f_{CLK} cycles between commands and between bytes within a command is required, starting from the last SCLK rising edge of one command to the first SCLK rising edge of the following command. The required delay is shown in Figure 58.



(1) $t_{SCLKDLY}$ = 24 / f_{CLK} (min).

Figure 58. Consecutive Commands

8.5.1.1 SDATAC Requirements

In read-data-continuous mode, the ADS1283 places conversion data on the DOUT pin as SCLK is applied. As a result of the potential conflict between conversion data and register data placed on DOUT resulting from a RREG or RDATA operation, it is necessary to send a stop-read-data-continuous (SDATAC) command before a RREG or RDATA command. The SDATAC command disables the direct output of conversion data on the DOUT pin. $\overline{CS}$ = 1 cancels SDATAC mode; therefore, keep $\overline{CS}$ held low after sending the SDATAC command to the next RREG or RDATA command.

8.5.1.2 WAKEUP: Wake-Up From Standby Mode

The WAKEUP command is used to exit the standby mode. After sending this command, the time for the first data to be ready is illustrated in Figure 48 and Table 16. Sending this command during normal operation has no effect; for example, reading data by the read-data-continuous mode with DIN held low.

8.5.1.3 STANDBY: Standby Mode

The STANDBY command places the ADS1283 into standby mode. In standby, the device enters a reduced power state where a low quiescent current remains to keep the register settings and serial interface active. The ADC remains in standby mode until $\overline{CS}$ is taken high or the WAKEUP command is sent. For complete device shutdown, take the $\overline{PWDN}$ pin low (register settings are not saved). The operation of standby mode is shown in Figure 59.

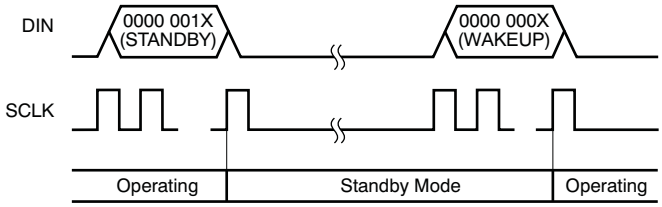


Figure 59. STANDBY Command Sequence

8.5.1.4 SYNC: Synchronize the Analog-to-Digital Conversion

The SYNC command synchronizes the analog-to-digital conversion. Upon receiving the command, the reading in progress is cancelled and the conversion process is restarted. In order to synchronize multiple ADS1283s, the command must be sent simultaneously to all devices. The SYNC pin must be held high during this command.

8.5.1.5 RESET: Reset the Device

The RESET command resets the registers to default values, enables read-data-continuous mode, and restarts the conversion process. The RESET command is functionally equivalent to taking the $\overline{RESET}$ pin low. See Figure 47 for the RESET command timing.

8.5.1.6 RDATAC: Read Data Continuous

The RDATAC command enables read-data-continuous mode (default mode). In this mode, conversion data is read from the device directly without the need to supply a data read command. Each time $\overline{DRDY}$ falls low, new data are available to read. See the *Read-Data-Continuous Mode* section for more details.

8.5.1.7 SDATAC: Stop Read Data Continuous

The SDATAC command stops read-data-continuous mode. Exit read-data-continuous mode before sending register and data read commands. The SDATAC command suppresses the $\overline{DRDY}$ output, but the ADS1283 continues conversions. Take $\overline{CS}$ high to cancel SDATAC mode.

8.5.1.8 RDATA: Read Data by Command

The RDATA command reads the conversion data. See the *Read-Data-By-Command Mode* section for more details.

8.5.1.9 RREG: Read Register Data

The RREG command is used to read single- or multiple-register data. The command consists of a two-byte opcode argument, followed by the output of register data. The first byte of the opcode includes the starting address, and the second byte specifies the number of registers to read minus one.

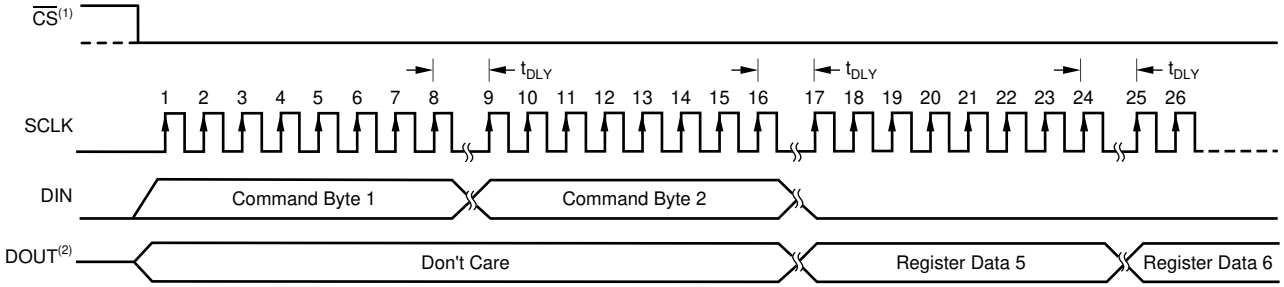
First command byte: 001r *rrrr*, where *rrrr* is the starting address of the first register.

Second command byte: 000n *nnnn*, where *nnnnn* is the number of registers to read minus one.

Starting with the 16th falling edge of SCLK, the register data appear on DOUT. Read the data on the 17th SCLK rising edge.

The RREG command is illustrated in Figure 60.

A delay of 24 f_{CLK} cycles is required between each byte transaction.



Example: Read six registers, starting at register 05h (OFC0)
Command Byte 1 = 0010 0101
Command Byte 2 = 0000 0101

(1) DOUT is in tristate when $\overline{CS}$ is high. $\overline{CS}$ can be tied low. See Figure 1 for $\overline{CS}$ low to SCLK rising edge time.

Figure 60. Read Register Data (Table 24 shows t_{DLY})

Table 24. t_{DRY} Value

PARAMETER	MIN
t_{DLY}	24 / f_{CLK}

8.5.1.10 WREG: Write to Register

The WREG command writes single- or multiple-register data. The command consists of a two-byte op-code argument followed by the input of register data. The first byte of the op-code contains the starting address and the second byte specifies the number of registers to write minus one.

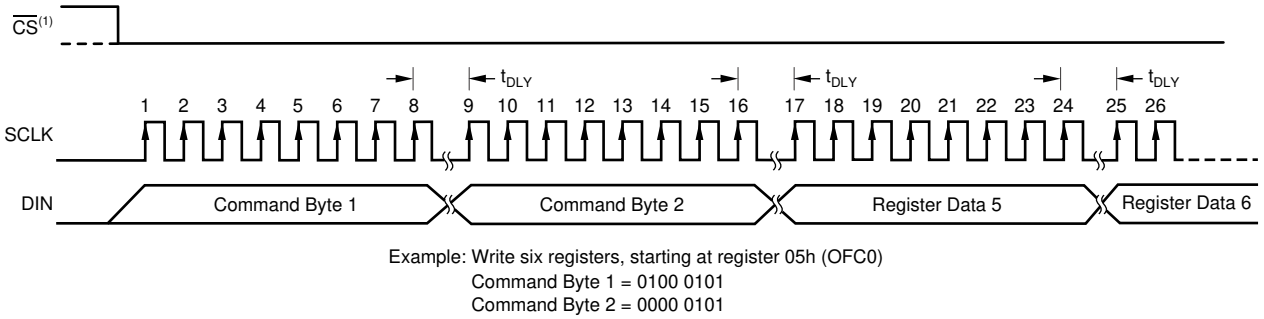
First command byte: 010r *rrrr*, where *rrrrr* is the starting address of the first register.

Second command byte: 000n *nnnn*, where *nnnnn* is the number of registers to write minus one.

Data byte(s): one or more register data bytes, depending on the number of registers specified.

Figure 61 illustrates the WREG command.

A delay of 24 f_{CLK} cycles is required between each byte transaction.



Example: Write six registers, starting at register 05h (OFC0)
Command Byte 1 = 0100 0101
Command Byte 2 = 0000 0101

(1) $\overline{CS}$ can be tied low. See Figure 1 for $\overline{CS}$ low to SCLK rising edge time.

Figure 61. Write Register Data (Table 24 shows t_{DLY})

8.5.1.11 OFSCAL: Offset Calibration

The OFSCAL command performs an offset calibration. The inputs to the converter (or the inputs to the external preamplifier) should be zeroed and allowed to stabilize before sending this command. The offset calibration register updates after this operation. See the *Calibration Commands* section for more details.

8.5.1.12 GANCAL: Gain Calibration

The GANCAL command performs a gain calibration. The inputs to the converter should have a stable dc input (typically full-scale, but not to exceed 106% full-scale). The gain calibration register updates after this operation. See the *Calibration Commands* section for more details.

8.6 Register Maps

Collectively, the registers contain all the information needed to configure the device, such as data rate, filter selection, calibration, and more. The registers are accessed by the RREG and WREG commands. The registers can be accessed individually or as a block of registers by sending or receiving consecutive bytes. After a register write operation, the ADC resets, resulting in an interruption of 63 readings.

Table 25. Register Map

ADDRESS	REGISTER	RESET VALUE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	ID_CFG	X0h	ID3	ID2	ID1	ID0	0	0	OFFSET1	OFFSET0
01h	CONFIG0	52h	SYNC	1	DR2	DR1	DR0	PHASE	FILTR1	FILTR0
02h	CONFIG1	08h	0	MUX2	MUX1	MUX0	CHOP	PGA2	PGA1	PGA0
03h	HPF0	32h	HPF07	HPF06	HPF05	HPF04	HPF03	HPF02	HPF01	HPF00
04h	HPF1	03h	HPF15	HPF14	HPF13	HPF12	HPF11	HPF10	HPF09	HPF08
05h	OFC0	00h	OFC07	OFC06	OFC05	OFC04	OFC03	OFC02	OFC01	OFC00
06h	OFC1	00h	OFC15	OFC14	OFC13	OFC12	OFC11	OFC10	OFC09	OFC08
07h	OFC2	00h	OFC23	OFC22	OFC21	OFC20	OFC19	OFC18	OFC17	OFC16
08h	FSC0	00h	FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00
09h	FSC1	00h	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
0Ah	FSC2	40h	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16

8.6.1 Register Descriptions

8.6.1.1 ID_CFG: ID_Configuration Register (address = 00h) [reset =x0h]

Figure 62. ID_CFG Register

7	6	5	4	3	2	1	0
ID3	ID2	ID1	ID0	0	0	OFFSET1	OFFSET0
R-xh	R-xh	R-xh	R-xh	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Bit[7:4] **ID[3:0]**

Factory-programmed identification bits (read-only). The ID bits are subject to change without notification.

Bit[3:2] **Reserved**

Always write 00

Bit[1:0] **OFFSET[1:0] (see *Offset* section)**

00: Disables offset (default)
01: Reserved
10: Offset = 100/PGA mV (all ADS1283 versions)
11: Offset = 75/PGA mV (ADS1283B only)

8.6.1.2 CONFIG0: Configuration Register 0 (address = 01h) [reset = 52h]

Figure 63. CONFIG0 Register

7	6	5	4	3	2	1	0
SYNC	1	DR2	DR1	DR0	PHASE	FILTR1	FILTR0
R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W -1h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Bit[7] **SYNC**

Synchronization mode bit.
0: Pulse-sync mode (default)
1: Continuous-sync mode

Bit[6] **RESERVED**

Always write 1

Bit[5:3] **DR[2:0]**

Data rate select bits.

000: 250 SPS
001: 500 SPS
010: 1000 SPS (default)
011: 2000 SPS
100: 4000 SPS

Bit[2] **PHASE**

FIR phase response bit.

0: Linear phase (default)
1: Minimum phase

Bit[1:0] **FILTR[1:0]**

Digital filter configuration bits.

00: Reserved
01: Sinc filter block only
10: Sinc + LPF filter blocks (default)
11: Sinc + LPF + HPF filter blocks

8.6.1.3 CONFIG1: Configuration Register 1 (address = 02h) [reset = 08h]

Figure 64. CONFIG1 Register

7	6	5	4	3	2	1	0
0	MUX2	MUX1	MUX0	CHOP	PGA2	PGA1	PGA0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Bit[7] **Reserved**

Always write 0

Bit[6:4] **MUX[2:0]**

MUX select bits.

000: AINP1 and AINN1 (default)
001: AINP2 and AINN2
010: Internal short through 400-Ω resistor
011: AINP1 and AINN1 connected to AINP2 and AINN2
100: External short to AINN2

Bit[3] **CHOP**

PGA chopping enable bit.

0: PGA chopping disabled
1: PGA chopping enabled (default)

Bit[2:0] **PGA[2:0]**

PGA gain select bits. Note that ADS1283A supports PGA gains of 1, 4, and 16 only.

000: G = 1 (default)
001: G = 2 (ADS1283 and ADS1283B only)
010: G = 4
011: G = 8 (ADS1283 and ADS1283B only)
100: G = 16
101: G = 32 (ADS1283 and ADS1283B only)
110: G = 64 (ADS1283 and ADS1283B only)

8.6.1.4 HPF0 and HPF1 Registers

These two bytes (high-byte and low-byte, respectively) set the corner frequency of the high-pass filter.

8.6.1.4.1 HPF0: High-Pass Filter Corner Frequency, Low Byte (address = 03h) [reset = 32h]

Figure 65. HPF0 Register

7	6	5	4	3	2	1	0
HPF07	HPF06	HPF05	HPF04	HPF03	HPF02	HPF01	HPF00
R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-1h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

8.6.1.4.2 HPF1: High-Pass Filter Corner Frequency, High Byte (address = 04h) [reset = 03h]

Figure 66. HPF1 Register

7	6	5	4	3	2	1	0
HPF15	HPF14	HPF13	HPF12	HPF11	HPF10	HPF09	HPF08
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	1R/W-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

8.6.1.5 OFC0, OFC1, OFC2 Registers

These three bytes set the offset calibration value.

8.6.1.5.1 OFC0: Offset Calibration, Low Byte (address = 05h) [reset = 00h]

Figure 67. OFC0 Register

7	6	5	4	3	2	1	0
OFC07	OFC06	OFC05	OFC04	OFC03	OFC02	OFC01	OFC00
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

8.6.1.5.2 OFC1: Offset Calibration, Mid Byte (address = 06h) [reset = 00h]

Figure 68. OFC1 Register

7	6	5	4	3	2	1	0
OFC15	OFC14	OFC13	OFC12	OFC11	OFC10	OFC09	OFC08
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

8.6.1.5.3 OFC2: Offset Calibration, High Byte (address = 07h) [reset = 00h]

Figure 69. OFC2 Register

7	6	5	4	3	2	1	0
OFC23	OFC22	OFC21	OFC20	OFC19	OFC18	OFC17	OFC16
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

8.6.1.6 FSC0, FSC1, FSC2 Registers

These three bytes set the full-scale calibration value.

8.6.1.6.1 FSC0: Full-Scale Calibration, Low Byte (address = 08h) [reset = 00h]

Figure 70. FSC0 Register

7	6	5	4	3	2	1	0
FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

8.6.1.6.2 FSC1: Full-Scale Calibration, Mid Byte (address = 09h) [reset = 00h]

Figure 71. FSC1 Register

7	6	5	4	3	2	1	0
FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

8.6.1.6.3 FSC2: Full-Scale Calibration, High Byte (address = 0Ah) [reset = 40h]

Figure 72. FSC2 Register

7	6	5	4	3	2	1	0
FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16
R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

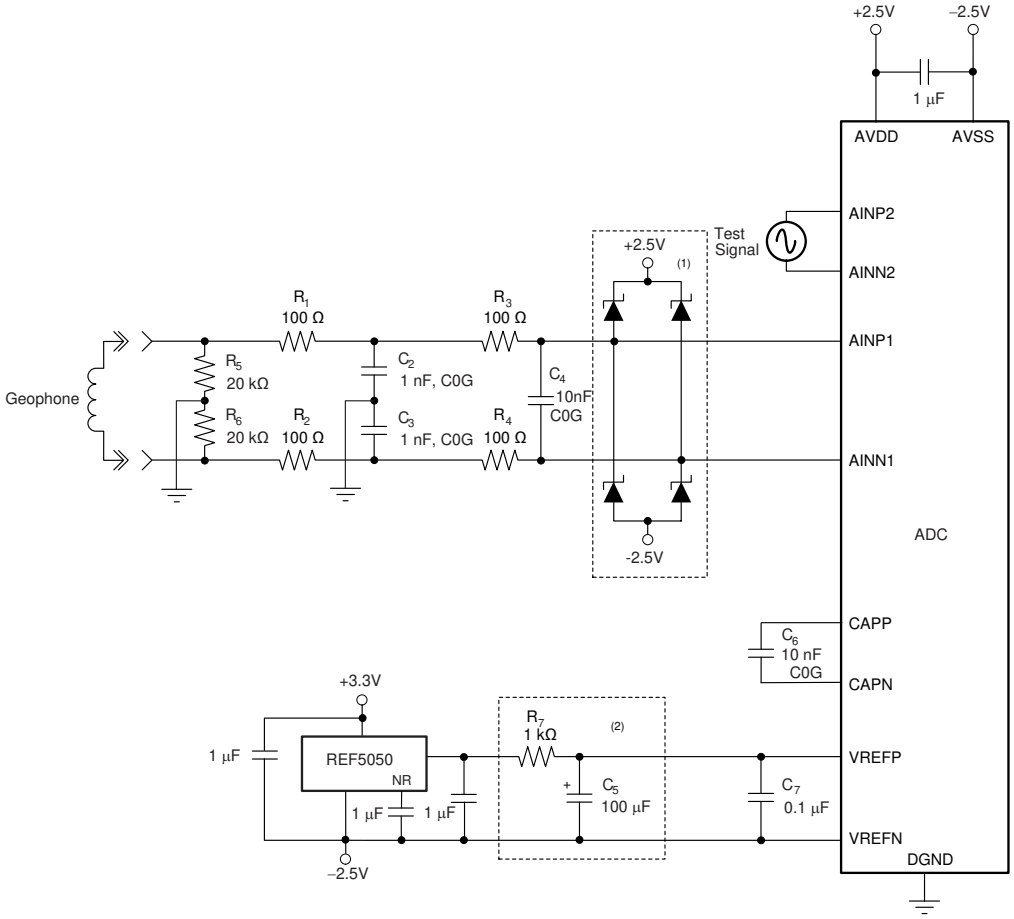
9.1 Application Information

The ADS1283 is a very high-resolution ADC. Optimal performance requires giving special attention to the support circuitry and printed circuit board (PCB) design. Locate noisy digital components (such as microcontrollers, oscillators, and so on) in an area of the PCB away from the converter and front-end components. Keep the digital current path short and separate from sensitive analog components by placing the digital components close to the power-entry point.

9.2 Typical Applications

9.2.1 Geophone Interface

A typical geophone front-end application is shown in Figure 73. The application diagram shows the ADS1283 operation with dual ±2.5-V analog supplies. The ADS1283 can also operate with a single 5-V analog supply.



(1) Optional external diode clamps.

(2) Optional reference noise filter.

Figure 73. Geophone Interface Application

Typical Applications (continued)

The geophone input signal is filtered by both a differential filter (components C_4 and R_1 to R_4) and by common-mode filters (components C_2, C_3 and R_1, R_2). The differential filter removes high-frequency normal-mode components from the input signal. The common-mode filters remove high-frequency components that are common to both input leads. The input filters are not required for all applications; check the system requirements for each application.

Resistors R_5 and R_6 bias the signal input to the midsupply point (ground). For single-supply operation, set the bias to a low impedance midsupply point (AVDD / 2 = 2.5 V).

Optional diode clamps protect the ADS1283 inputs from high-level voltage transients and overloads. The diodes provide additional protection if possible high-level input transients and surges exceed the ADC internal ESD diode rating.

The REF5050 5-V reference provides the reference to the ADC. An optional filter network (R_7 and C_5) reduces the in-band reference noise for improved dynamic performance. However, the RC filter network increases the filter settling-time (from seconds to possibly minutes) depending on the dielectric absorption properties of capacitor C_5. Capacitor C_7 is mandatory and provides high-frequency bypassing of the reference inputs; place C_7 as close as possible to the ADS1283 pins. Resistor R_7 (1 kΩ) results in a 1% systematic gain error. Multiple ADCs can share a single reference, but if shared, use independent reference filters for each ADC.

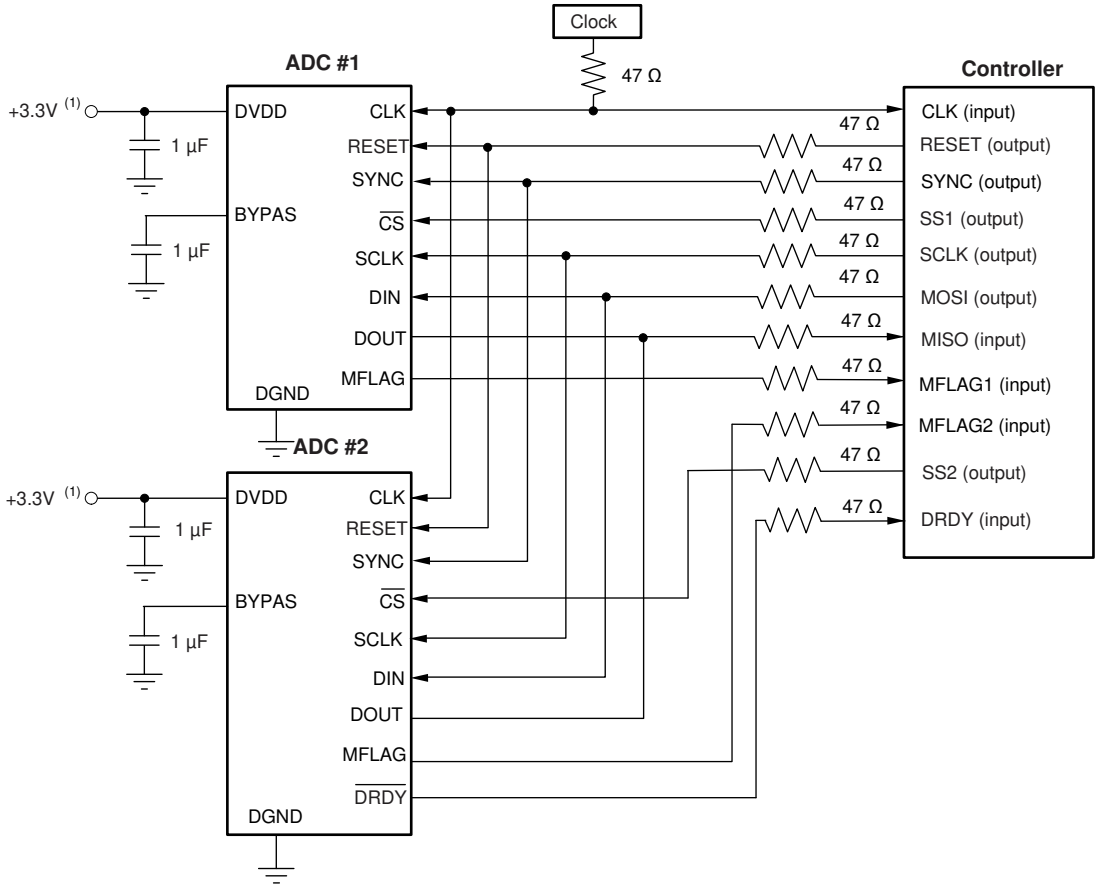
As an alternative, the REF5045 (4.5 V) reference can be used. The REF5045 reference has the advantage of operating directly from the 5-V (total) power supply; however, the 4.5-V reference reduces signal range by 10% and results in a 1-dB loss of SNR.

Capacitor C_6 (10 nF) filters the PGA output glitches caused by sampling of the modulator. This capacitor also forms an antialias filter with a low-pass cutoff frequency of 26 kHz.

Typical Applications (continued)

9.2.2 Digital Interface

Figure 74 shows the digital connection to a controller (field programmable gate array or microcontroller). In this example, two ADCs are shown connected to one controller. The ADCs share the same serial interface (SCLK, DIN, and DOUT). The ADC is selected for communication by strobing each $\overline{CS}$ low. The $\overline{DRDY}$ output from both ADCs can be used; however, when the devices are synchronized, the $\overline{DRDY}$ output from only one device is sufficient.



(1) For DVDD < 2.25 V, tie DVDD and BYPASS together. see the *DVDD Power Supply* section.

Figure 74. Controller Interface with Dual ADCs

The modulator overrange flag (MFLAG) from each device ties to the controller input. For synchronization, connect all ADCs to the same SYNC signal. For reset, either connect all ADCs to the same RESET signal or connect the ADCs to individual RESET signals.

Avoid ringing on the digital inputs to the ADCs. Place 47-Ω resistors in series with the digital traces to help reduce ringing by controlling impedances. Place the resistors at the source (driver) end of the trace. Do not float unused digital inputs; tie them to DVDD or GND.

9.3 Initialization Set Up

After reset or power-on, configure the registers using the following procedure:

1. **Reset the serial interface.** Before using the serial interface, it may be necessary to recover the serial interface (undefined I/O power-up sequencing may cause a false SCLK to occur). To reset the interface, toggle the $\overline{CS}$ pin high then low, or toggle the $\overline{RESET}$ pin high then low, or when in read-data-continuous mode, hold SCLK low for 64 $\overline{DRDY}$ periods.
2. **Configure the registers.** The registers are configured by either writing to them individually or as a group, and can be configured in either mode. To cancel read-data-continuous mode, send the SDATAC command before register read and write operations .
3. **Verify register data.** For verification of device communications, read back the register.
4. **Set the data mode.** After register configuration, configure the device for read-data-continuous mode by executing the RDATAC command, or configure for read-data-by-command mode (set in step 2, by the SDATAC command).
5. **Synchronize readings.** Whenever SYNC is high, the ADS1283 freely runs the data conversions. To resynchronize the conversions in pulse-sync mode, take SYNC low and then high. In continuous-sync mode, apply the synchronizing clock to the SYNC pin with a clock period equal to multiples of the ADC conversion period.
6. **Read data.** If read-data-continuous mode is active, the data are read directly after $\overline{DRDY}$ falls by applying SCLK pulses. If the read-data-continuous mode is inactive, the data can only be read by executing the RDATA command. The RDATA command must be sent in this mode to read each conversion result.

10 デバイスおよびドキュメントのサポート

10.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

10.3 商標

E2E is a trademark of Texas Instruments.
SPI is a trademark of Motorola Inc.
All other trademarks are the property of their respective owners.

10.4 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

10.5 Glossary

SLYZ022 — *TI Glossary*.

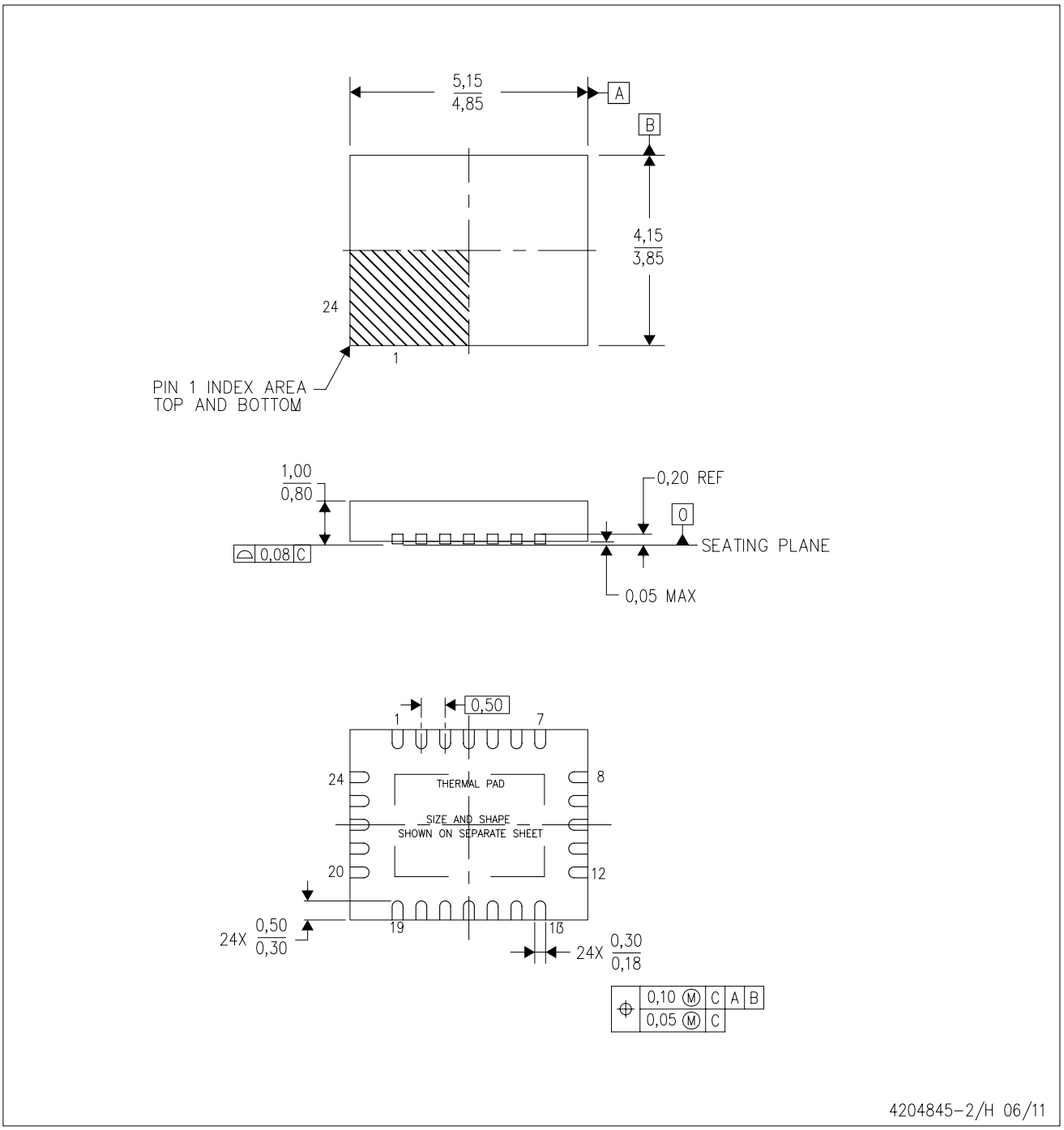
This glossary lists and explains terms, acronyms, and definitions.

11 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

MECHANICAL DATA

RHF (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

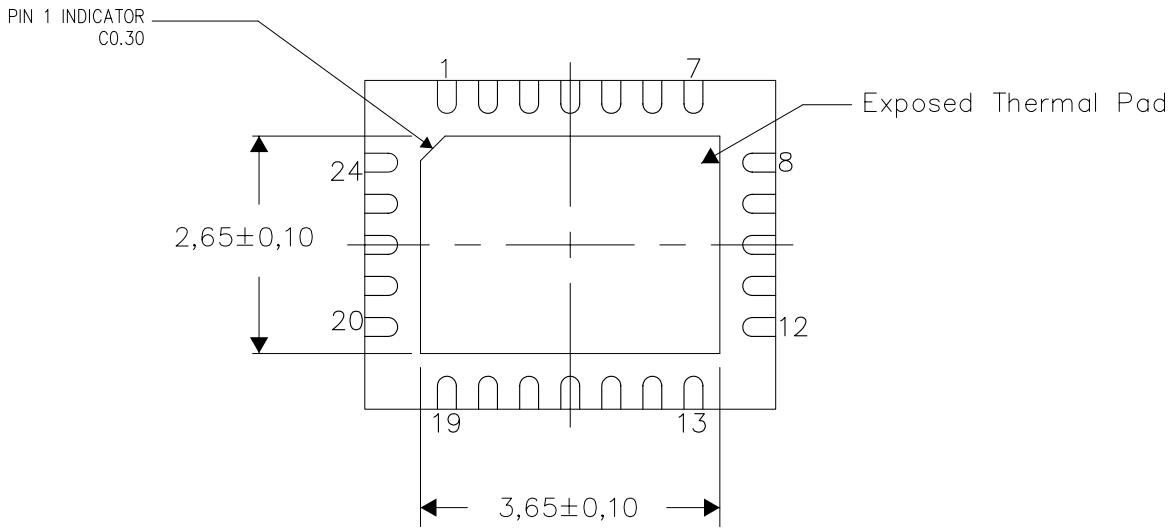
RHF (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

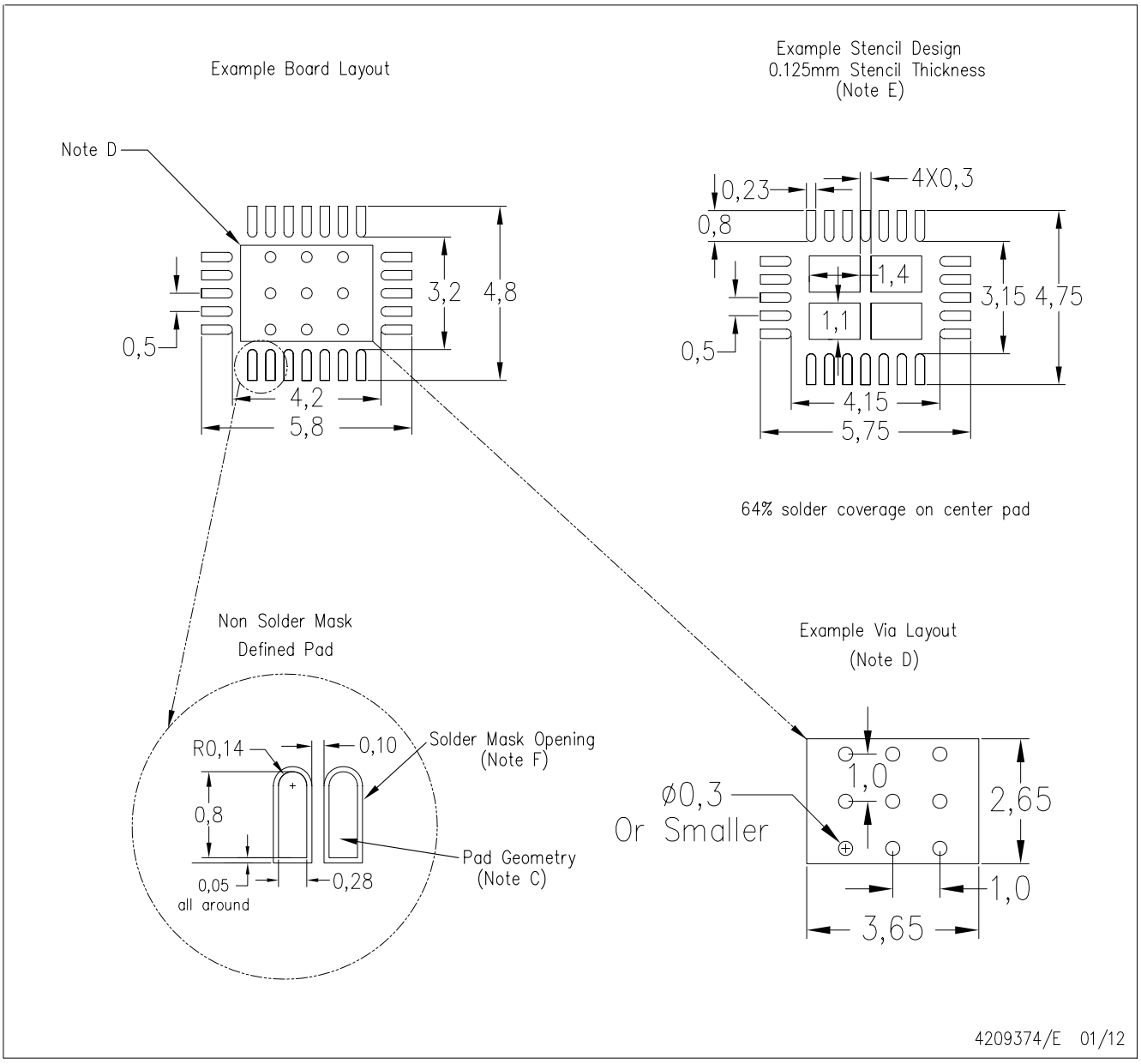
Exposed Thermal Pad Dimensions

4206360–3/J 01/12

NOTE: All linear dimensions are in millimeters

LAND PATTERN DATA

RHF (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1283AIRHFR	ACTIVE	VQFN	RHF	24	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS 1283A	Samples
ADS1283AIRHFT	ACTIVE	VQFN	RHF	24	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS 1283A	Samples
ADS1283BIRHFR	ACTIVE	VQFN	RHF	24	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS 1283B	Samples
ADS1283BIRHFT	ACTIVE	VQFN	RHF	24	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS 1283B	Samples
ADS1283IRHFR	ACTIVE	VQFN	RHF	24	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS 1283	Samples
ADS1283IRHFT	ACTIVE	VQFN	RHF	24	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS 1283	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

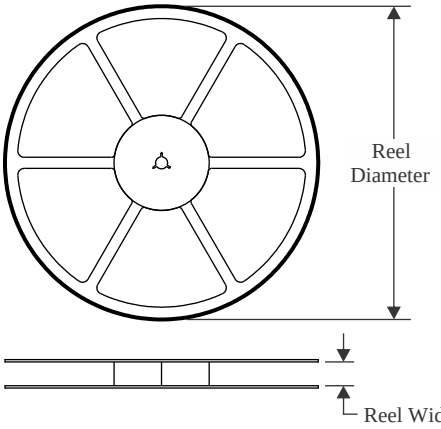
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

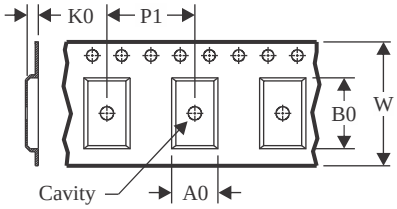
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

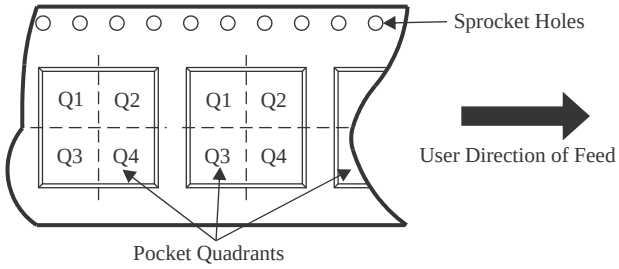


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

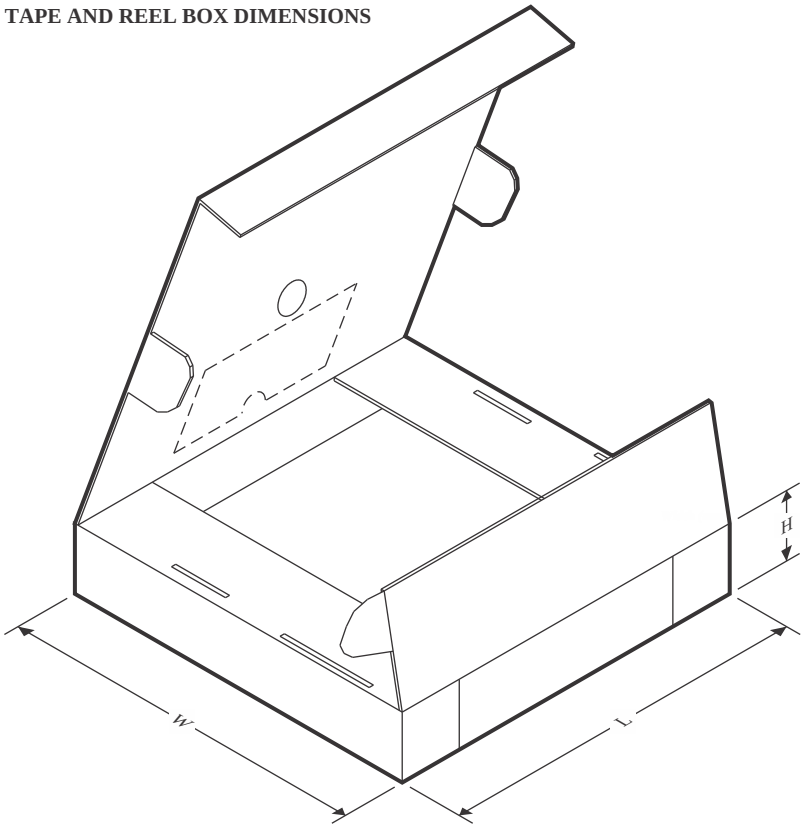
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1283AIRHFR	VQFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
ADS1283AIRHFR	VQFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
ADS1283AIRHFT	VQFN	RHF	24	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
ADS1283AIRHFT	VQFN	RHF	24	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
ADS1283BIRHFR	VQFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
ADS1283BIRHFT	VQFN	RHF	24	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
ADS1283IRHFR	VQFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
ADS1283IRHFR	VQFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
ADS1283IRHFT	VQFN	RHF	24	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
ADS1283IRHFT	VQFN	RHF	24	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

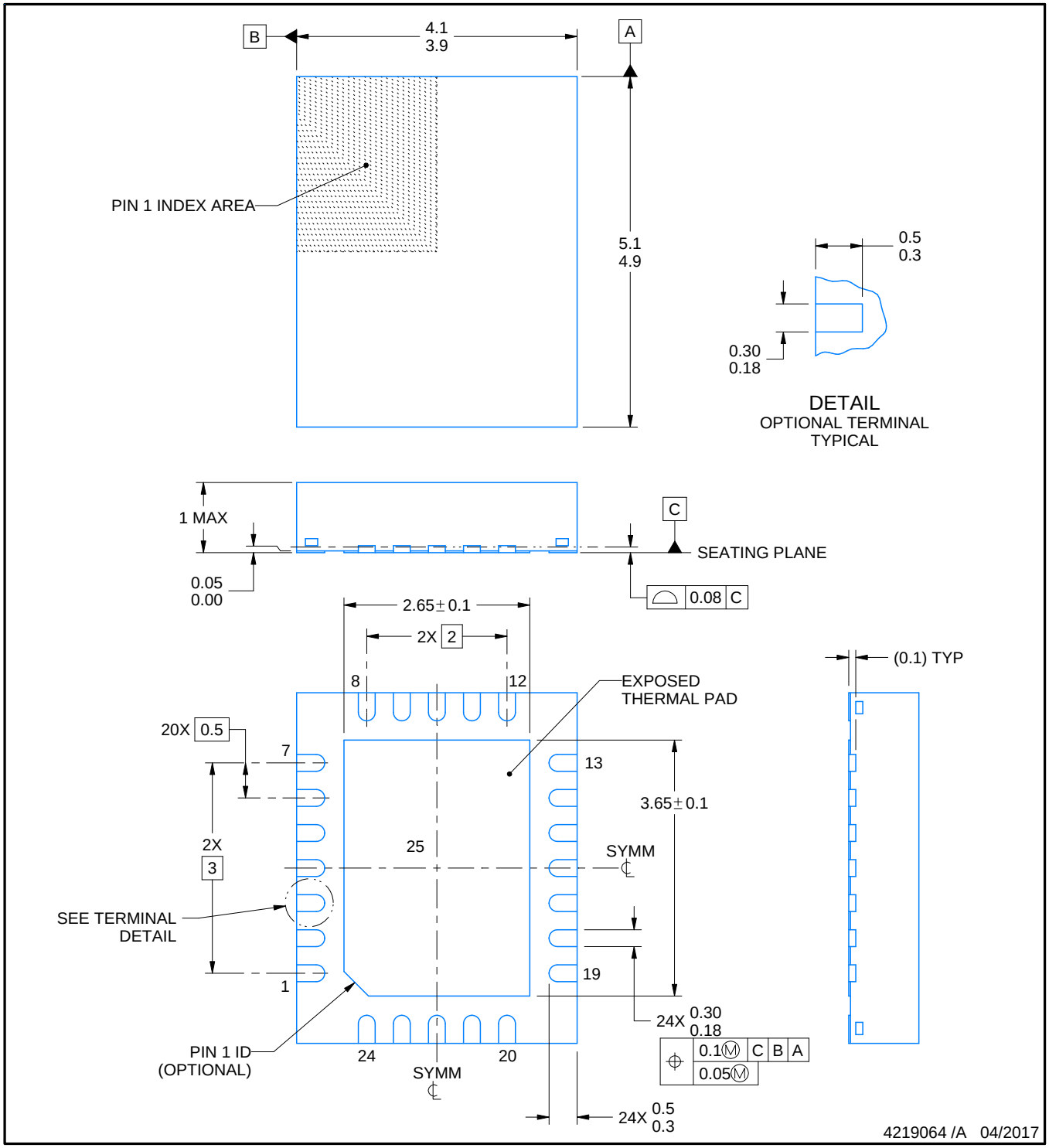
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1283AIRHFR	VQFN	RHF	24	3000	367.0	367.0	35.0
ADS1283AIRHFR	VQFN	RHF	24	3000	346.0	346.0	33.0
ADS1283AIRHFT	VQFN	RHF	24	250	210.0	185.0	35.0
ADS1283AIRHFT	VQFN	RHF	24	250	210.0	185.0	35.0
ADS1283BIRHFR	VQFN	RHF	24	3000	346.0	346.0	33.0
ADS1283BIRHFT	VQFN	RHF	24	250	210.0	185.0	35.0
ADS1283IRHFR	VQFN	RHF	24	3000	367.0	367.0	35.0
ADS1283IRHFR	VQFN	RHF	24	3000	346.0	346.0	33.0
ADS1283IRHFT	VQFN	RHF	24	250	210.0	185.0	35.0
ADS1283IRHFT	VQFN	RHF	24	250	210.0	185.0	35.0

PACKAGE OUTLINE

RHF0024A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

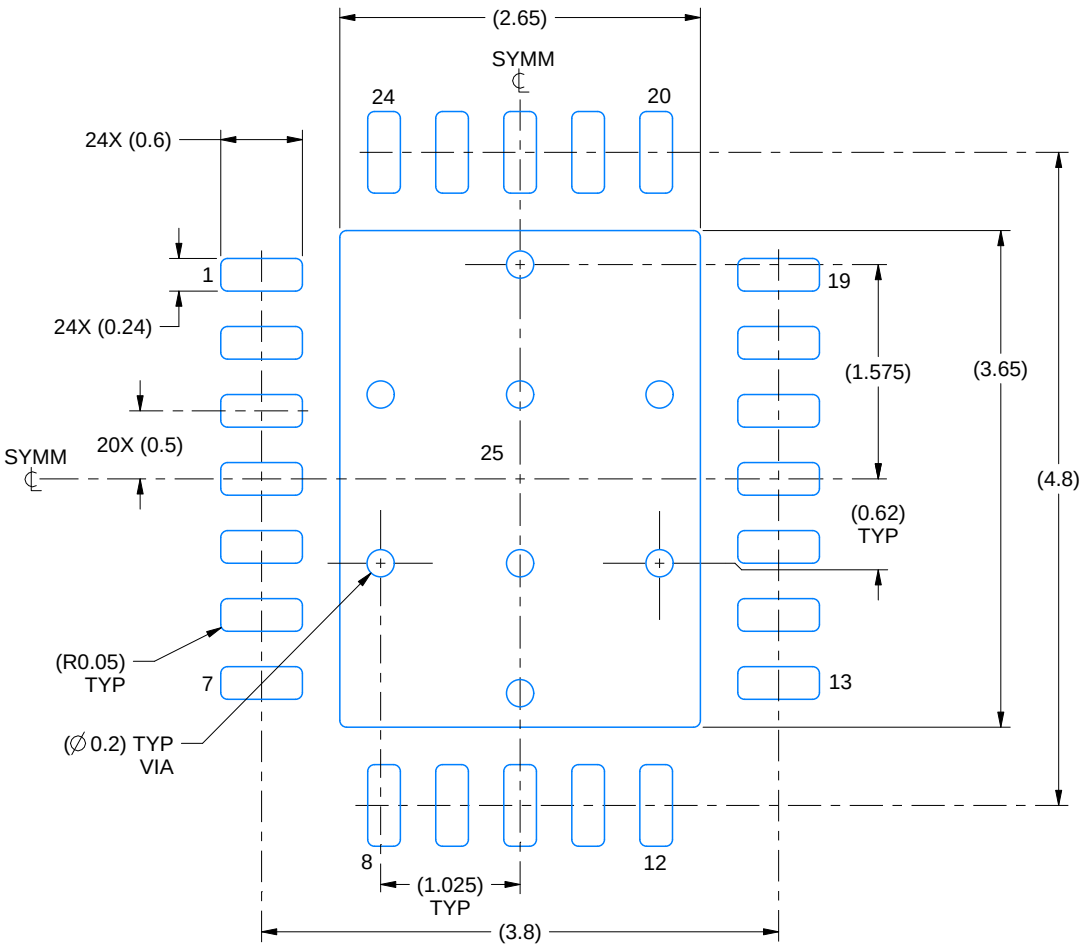
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

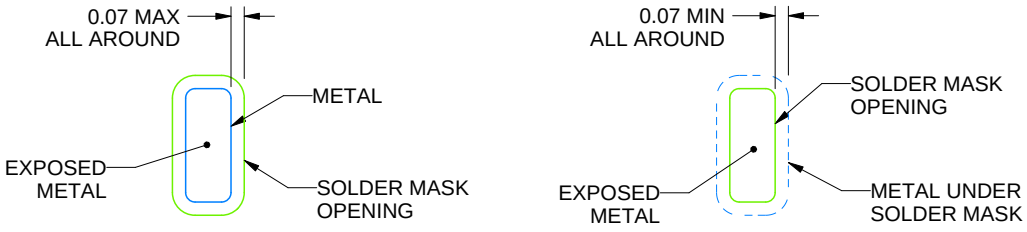
RHF0024A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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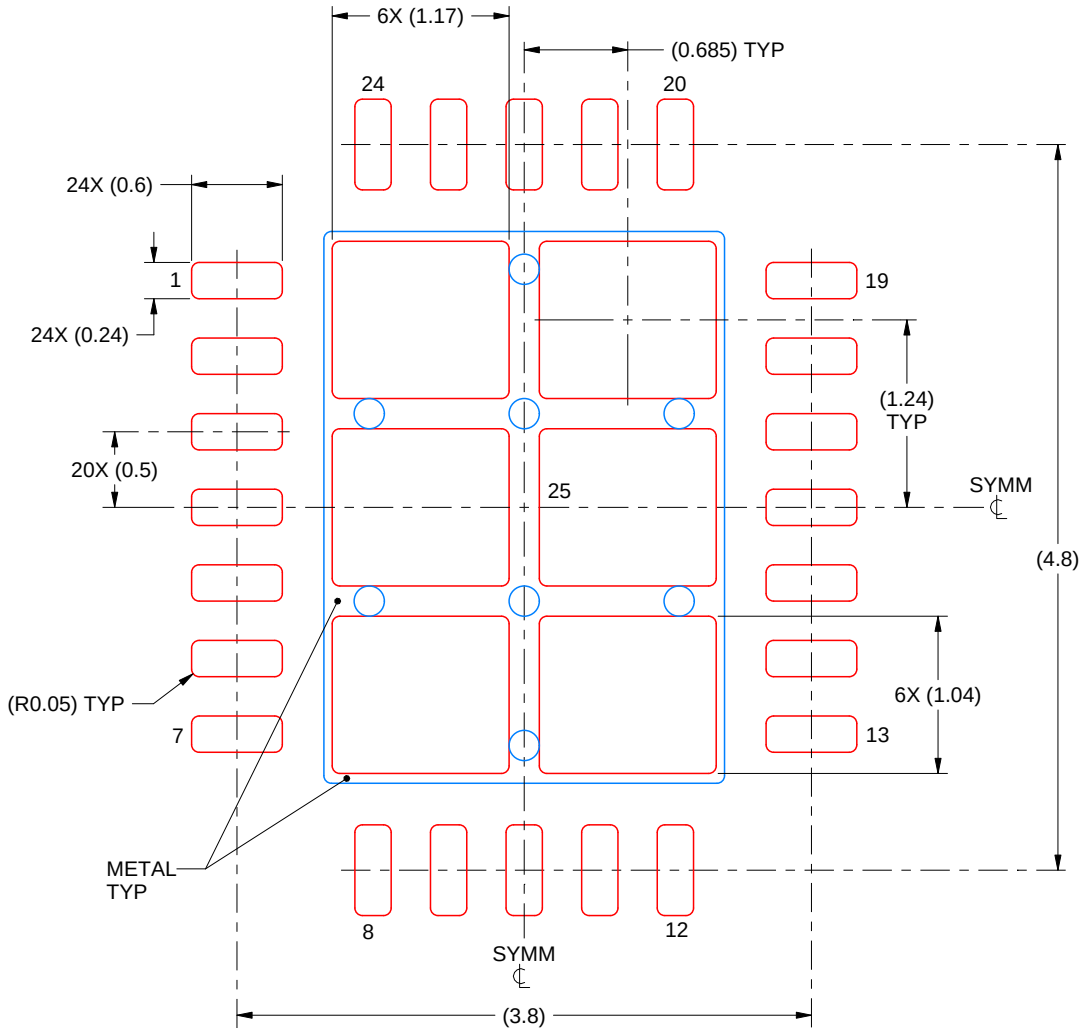
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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